

# Attention

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**For additional information, please contact Jim Beneke at Avnet ([jim.beneke@avnet.com](mailto:jim.beneke@avnet.com)).**



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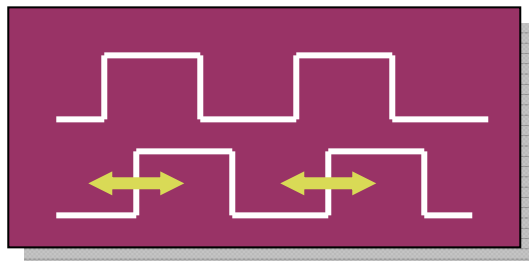
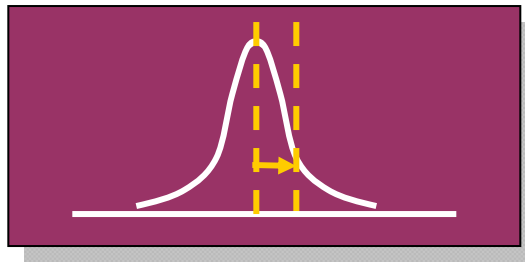
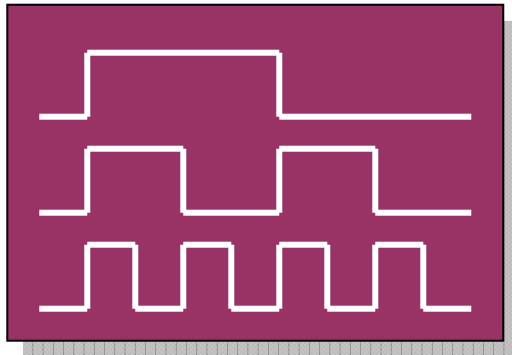
# 2009 Xfest

High Speed Clocking:  
Challenges, Pitfalls, and Solutions

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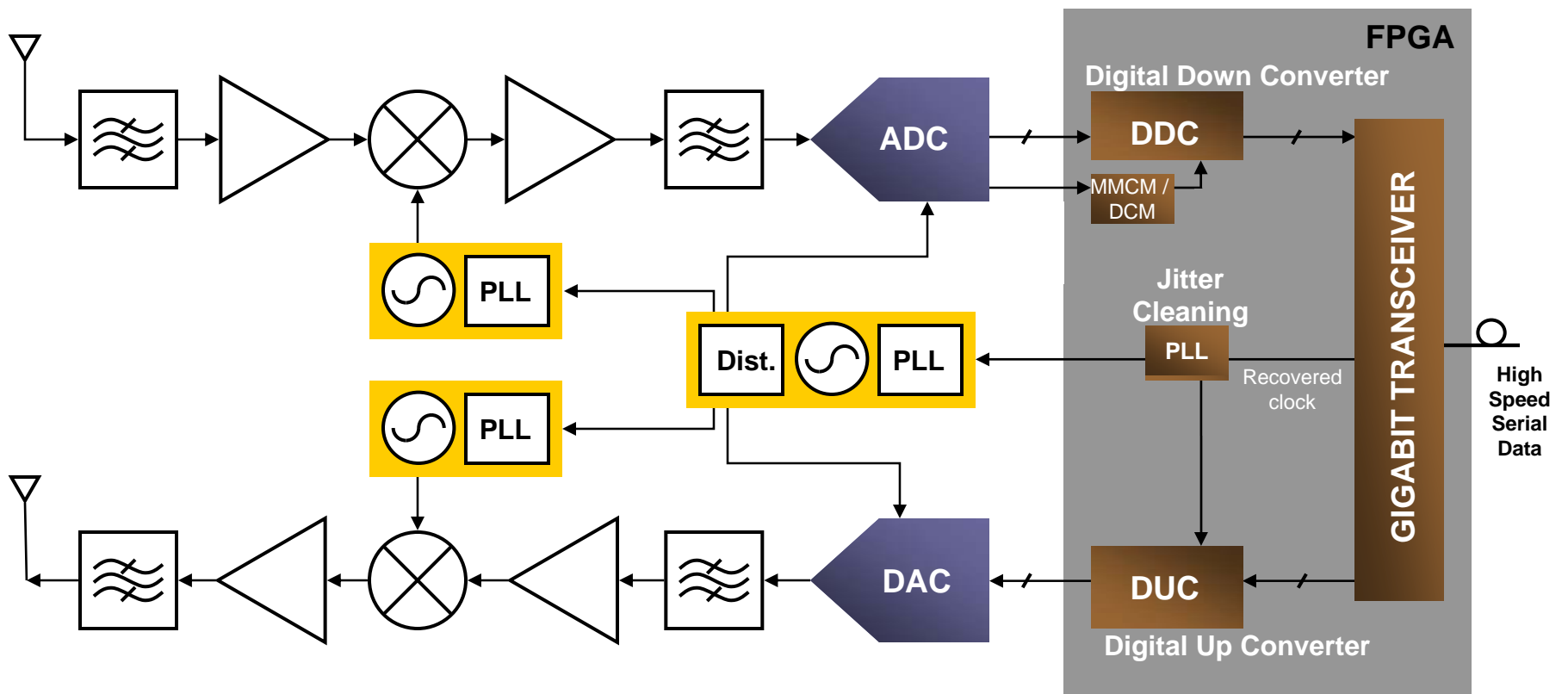
- **Understand high-speed clocking requirements at the system level**
- **Introduce analysis techniques of high-speed clocking**
- **Demonstrate industry-leading high-speed clocking solutions**

- **System-Level Clocking Overview**
- **High-Performance Clock Generators**
- **Xilinx® FPGA Clocking Resources**
- **Case Studies**
- **Demo**



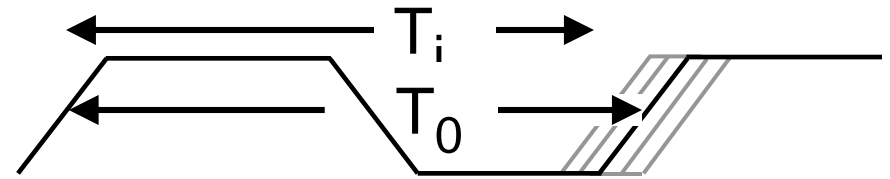
- **Modern applications have complex clocking requirements:**
  - Extremely high performance clock signals
  - Support for multiple frequency domains across a wide frequency range
  - De-skewing of clocks relative to one another
  - Low Jitter and precise duty cycle to maintain the widest possible data valid window
  - Lowest possible system power
  - The perfect balance of resources at the right cost

- Clock quality has direct impact on system performance



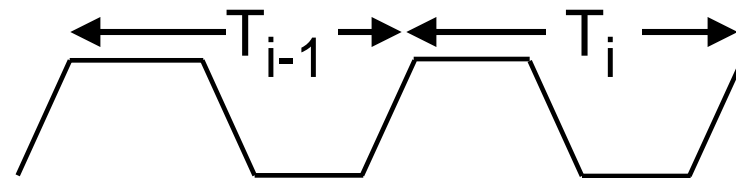
- **Period Jitter  $J_{T_0RMS}$**

- Deviation in clock period (from ideal  $T_0$ ) over many samples

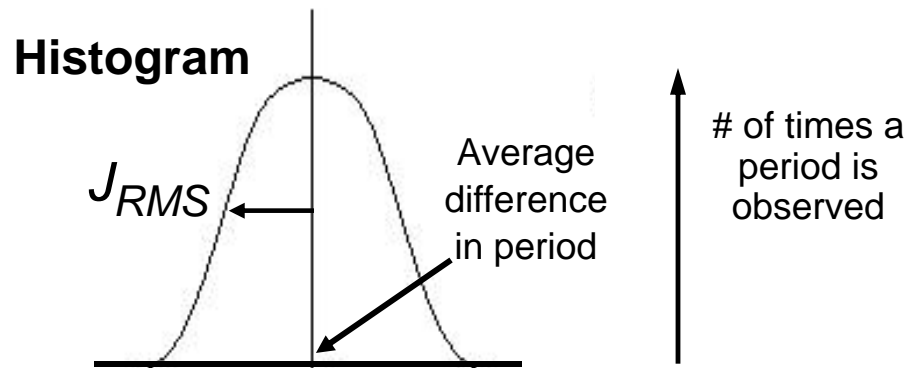


- **Cycle-to-Cycle Jitter  $J_{CCRMS}$**

- Difference in two consecutive periods (over many samples of consecutive periods)

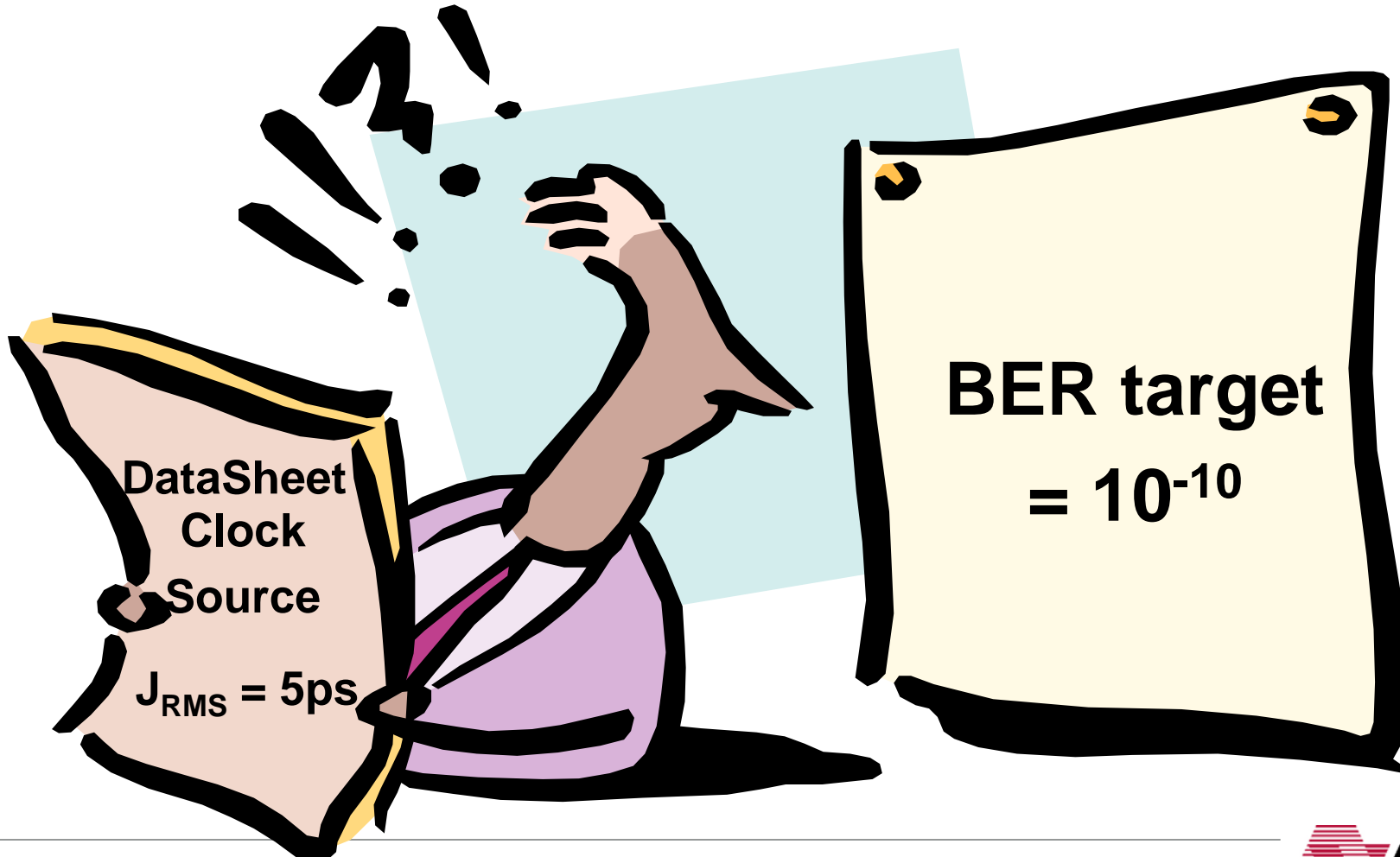
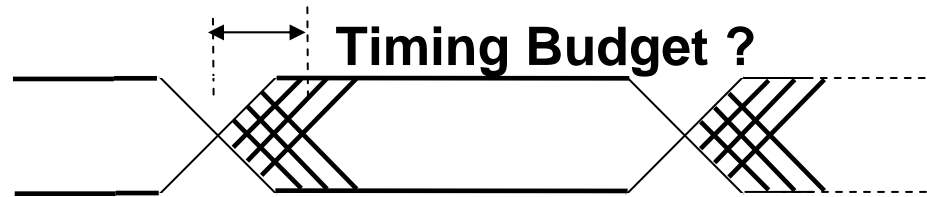


- **Equivalent to standard deviation  $\sigma$  of Gaussian distribution**



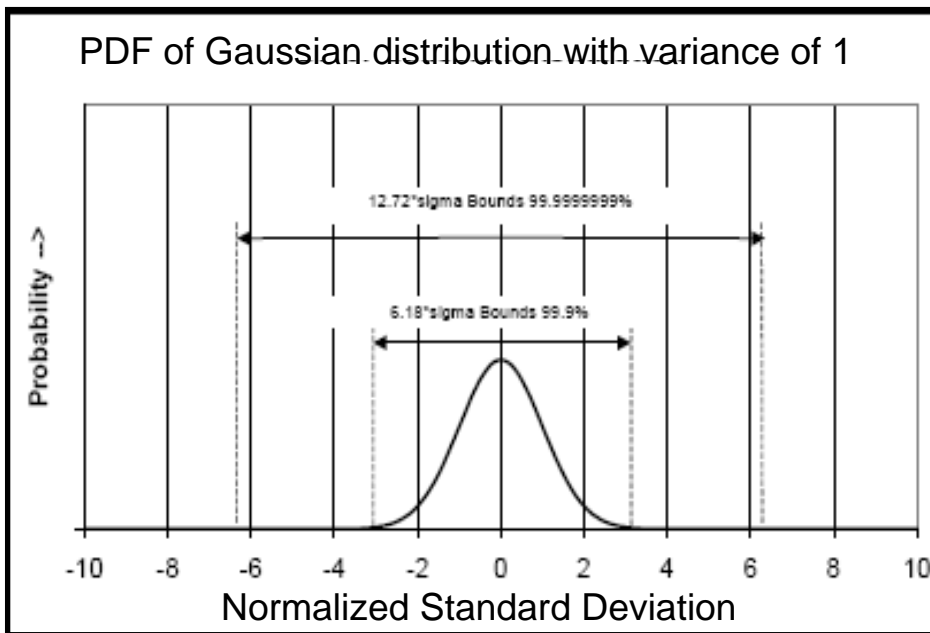
$$J_{T_0RMS} = \sqrt{\frac{1}{i_{tot}} \cdot \sum_{i=1}^{i_{tot}} (T_i - T_0)^2}$$

$$J_{CCRMS} = \sqrt{\frac{1}{i_{tot}} \cdot \sum_{i=1}^{i_{tot}} (T_i - T_{i-1})^2}$$



- Peak-to-peak jitter ( $J_{p-p}$ ) degrades timing margin
- $J_{p-p}$  = worst-case longest clock period – shortest
- PDF bounds  $J_{p-p}$  according to bit-error rate (BER)

$$BER = \frac{1}{2} \operatorname{erfc}(\sqrt{2} * \alpha)$$



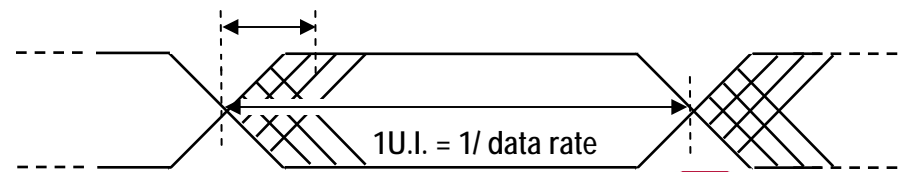
**Ex: BER target =  $10^{-10}$**

**$J_{RMS} = 5\text{ps}$**

**From erfc table find  $\alpha = 12.723$**

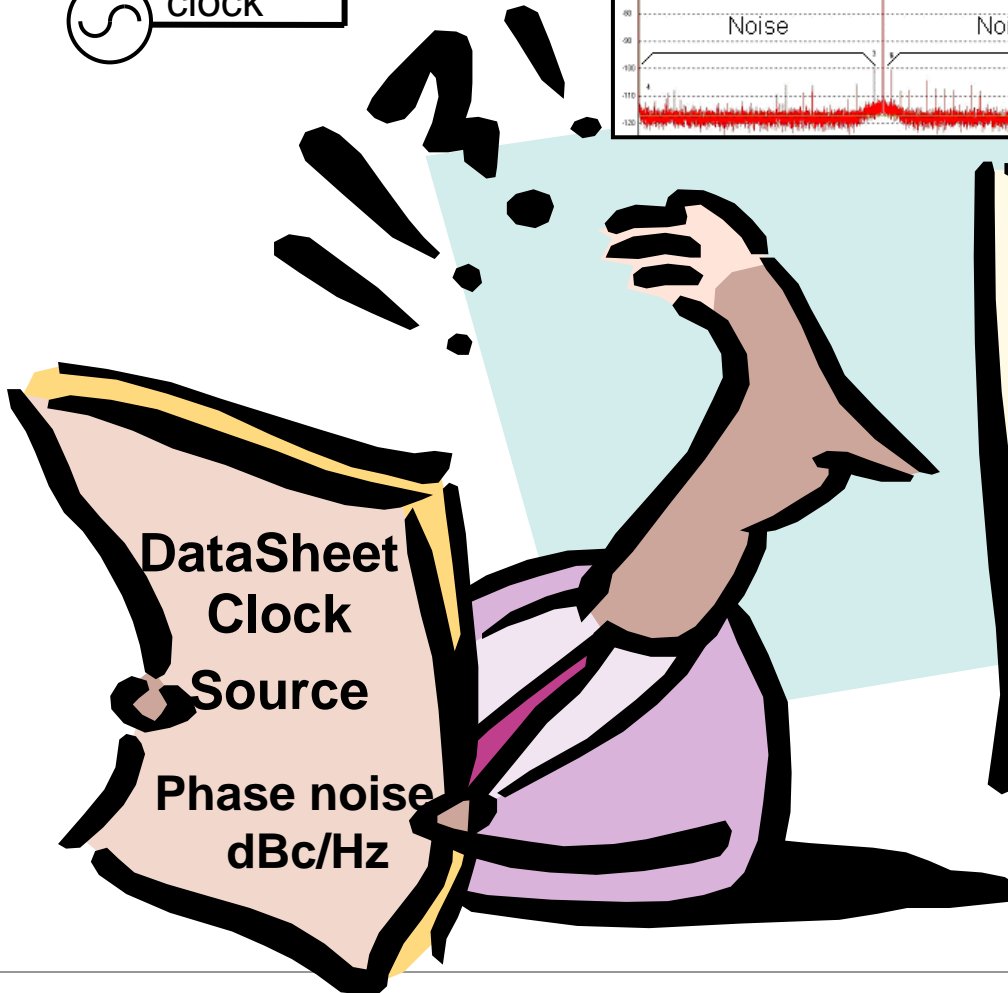
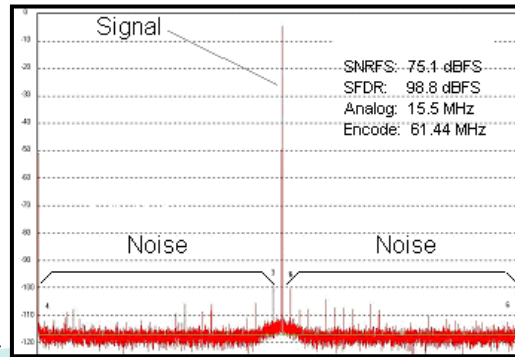
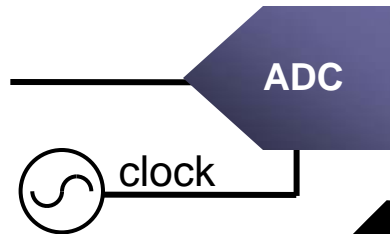
**$J_{p-p} = \alpha * J_{RMS}$**

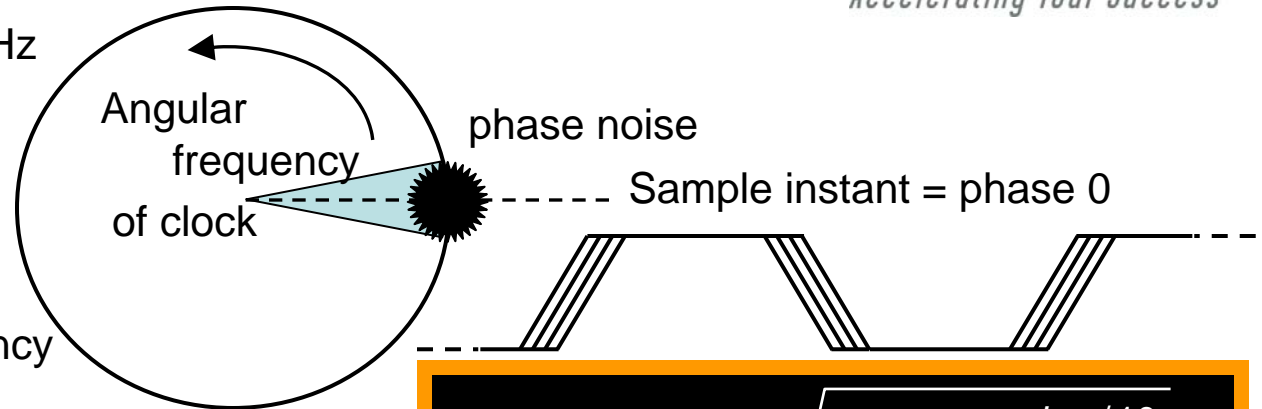
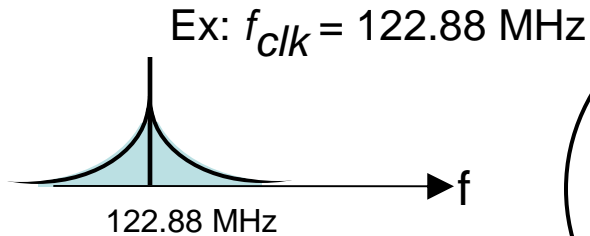
**$= 63\text{ ps}$**



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## Signal to Noise Ratio (SNR)



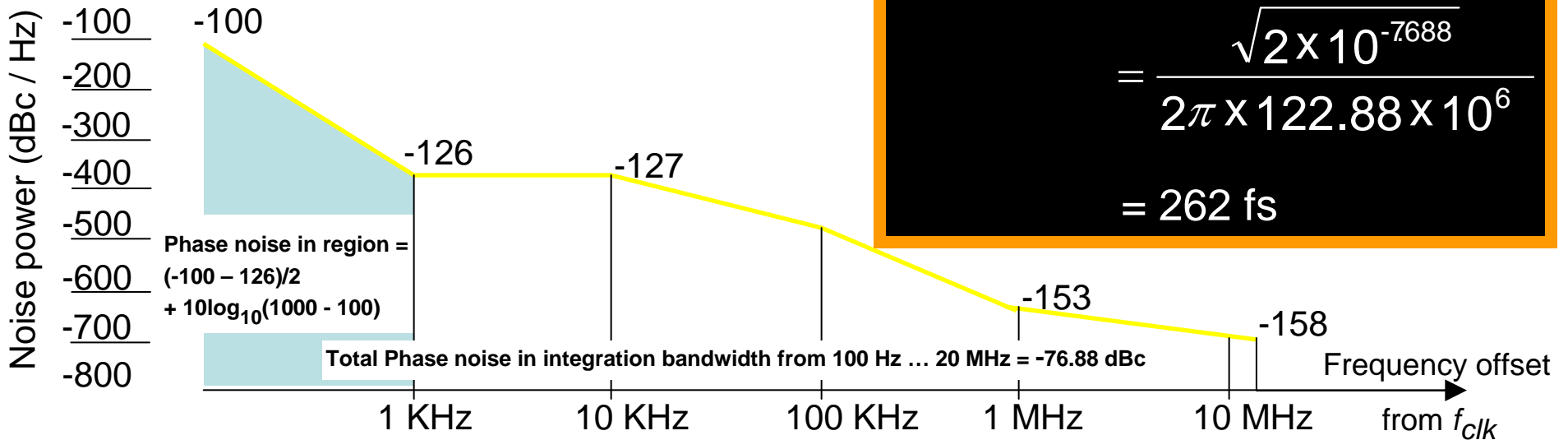


- Deviation from center frequency
  - Ex. 122.88 MHz
- Evaluated with a spectrum analyzer
- Measured in dBc/Hz

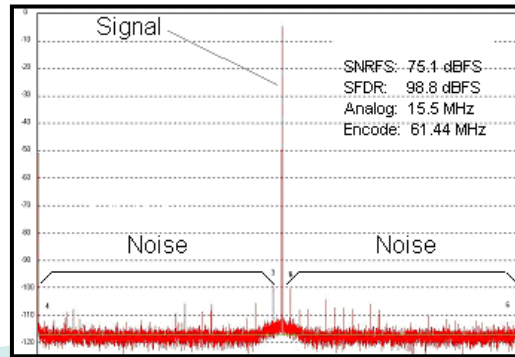
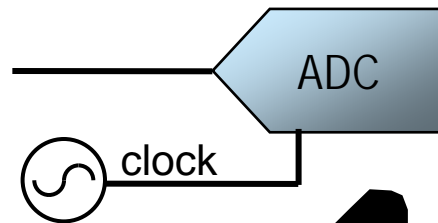
$$J_{T0}RMS = \frac{\sqrt{2 \times 10^{noise / 10}}}{2\pi f_{clk}}$$

$$= \frac{\sqrt{2 \times 10^{-76.88}}}{2\pi \times 122.88 \times 10^6}$$

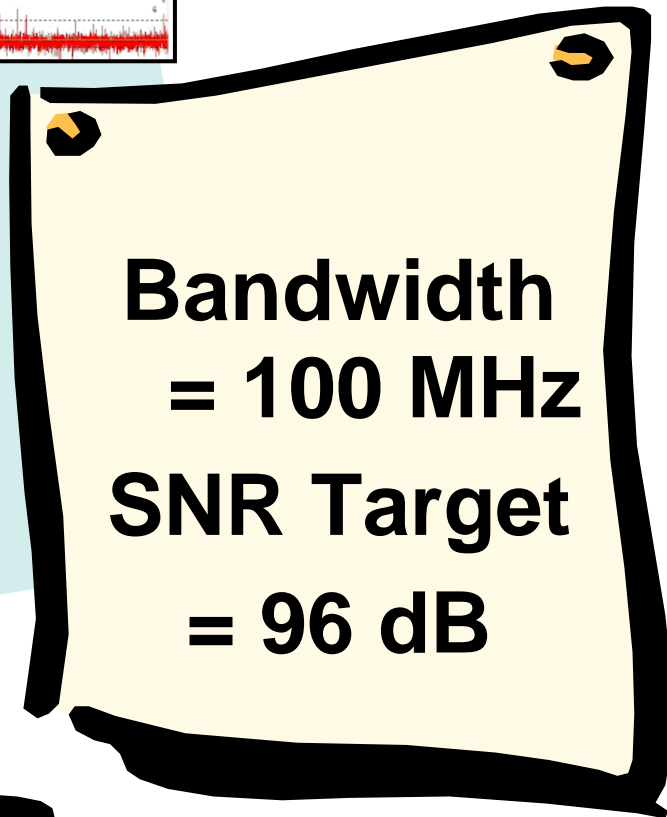
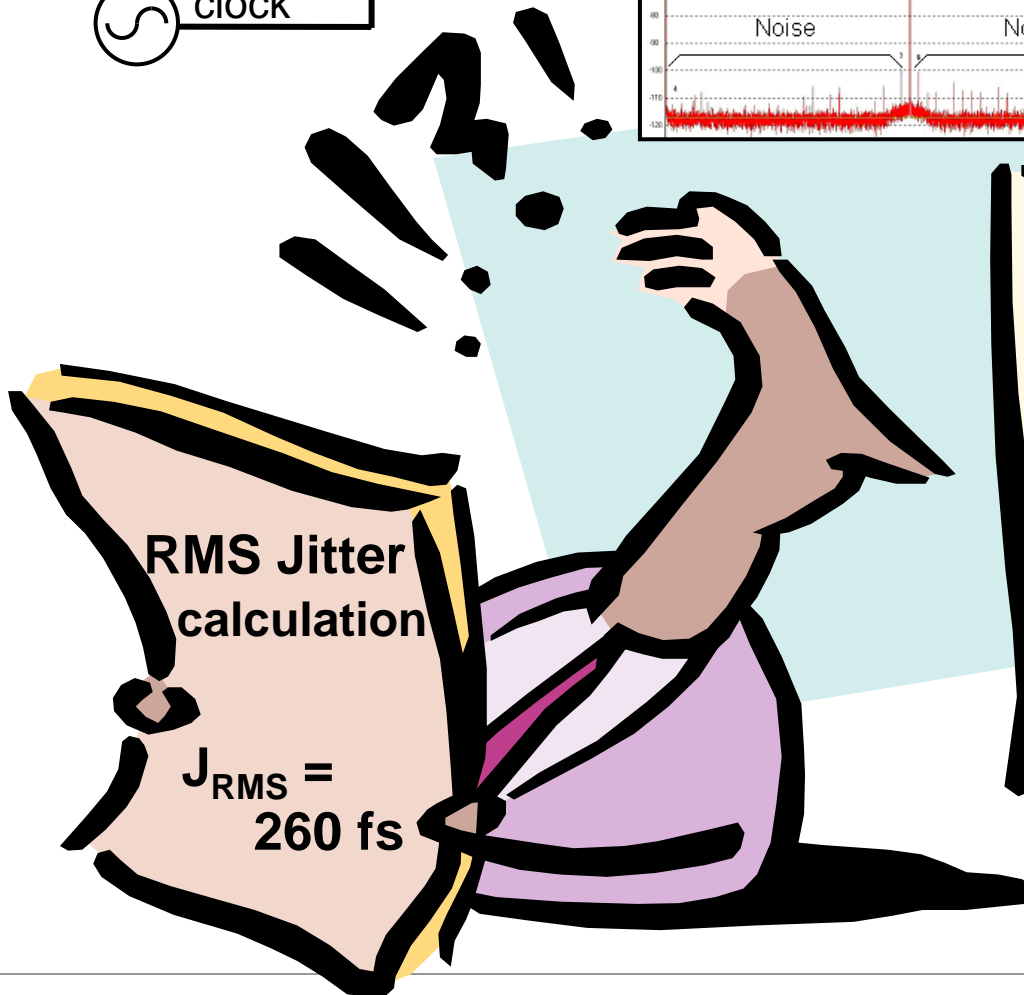
$$= 262 \text{ fs}$$



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## Signal to Noise Ratio (SNR)

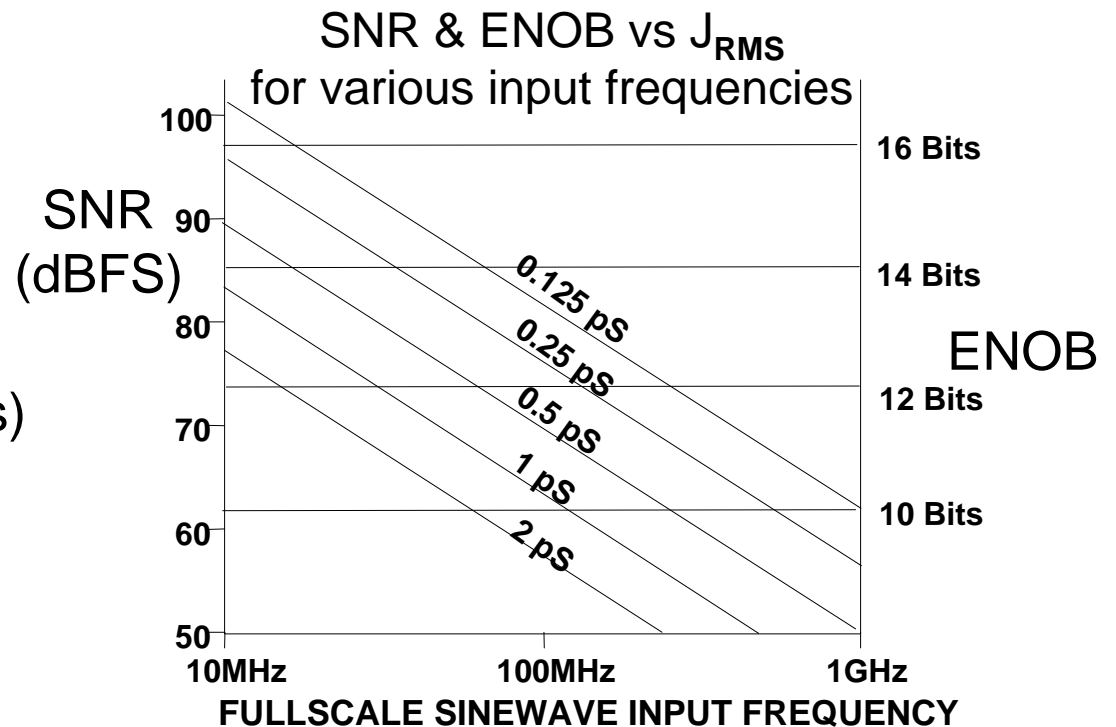
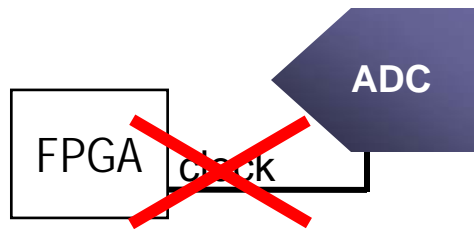


- ADC applications require 2-3 orders of magnitude better jitter than high-speed digital applications
- Random and deterministic jitter degrades SNR of an ADC (DAC)
- Deterministic jitter degrades Spurious Free Dynamic Range (SFDR) of an ADC (DAC)

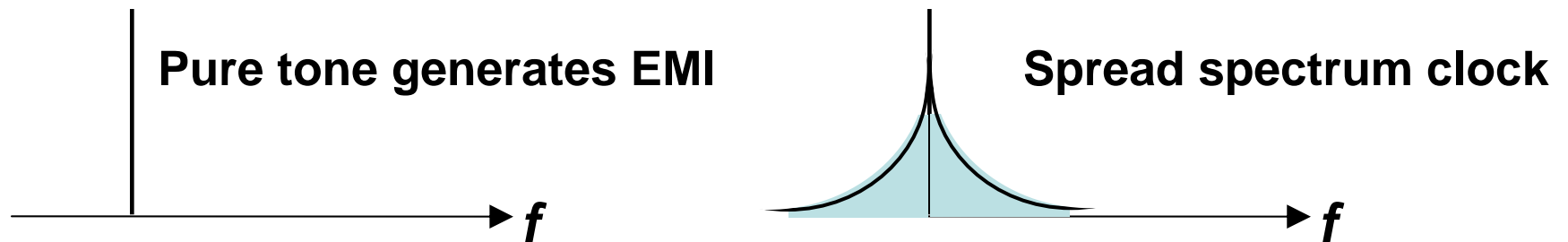
$$SNR = 20 \log_{10} \left[ \frac{1}{2\pi f J_{RMS}} \right]$$

$J_{RMS}$  = sample clock RMS jitter (ps)

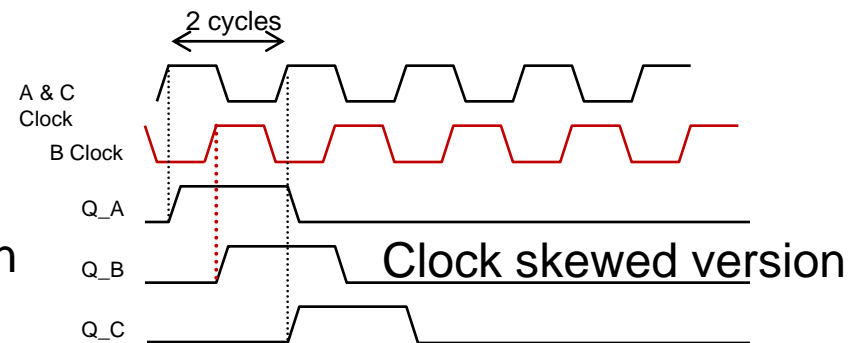
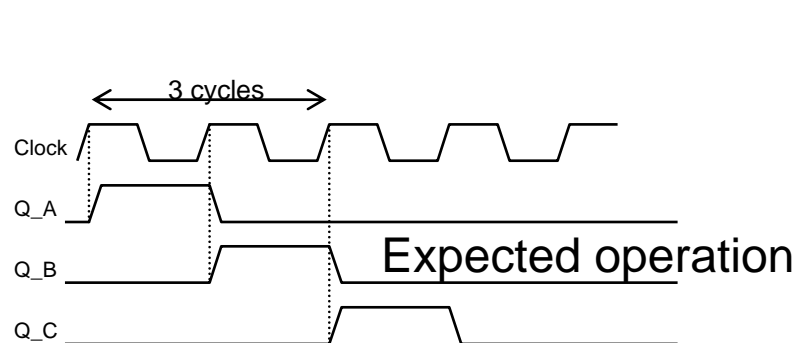
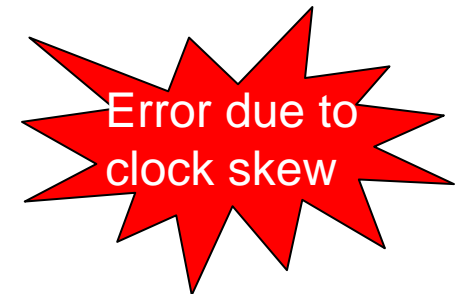
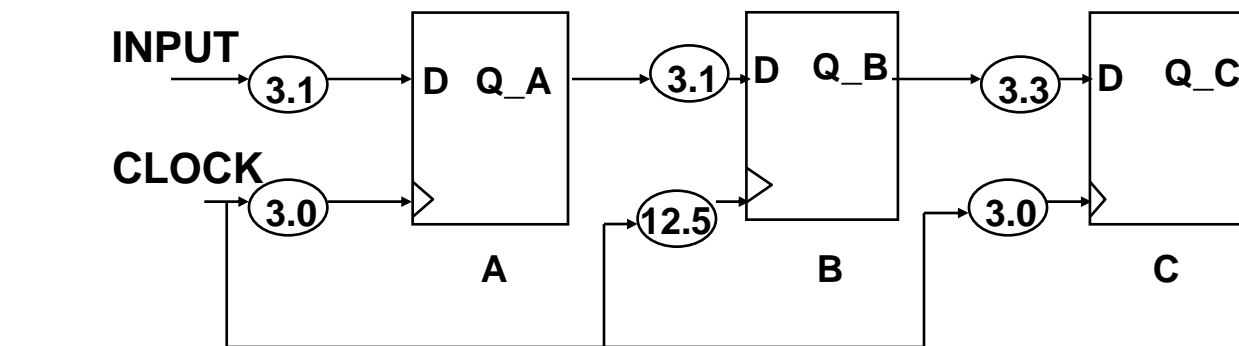
ENOB = Effective Number of Bits



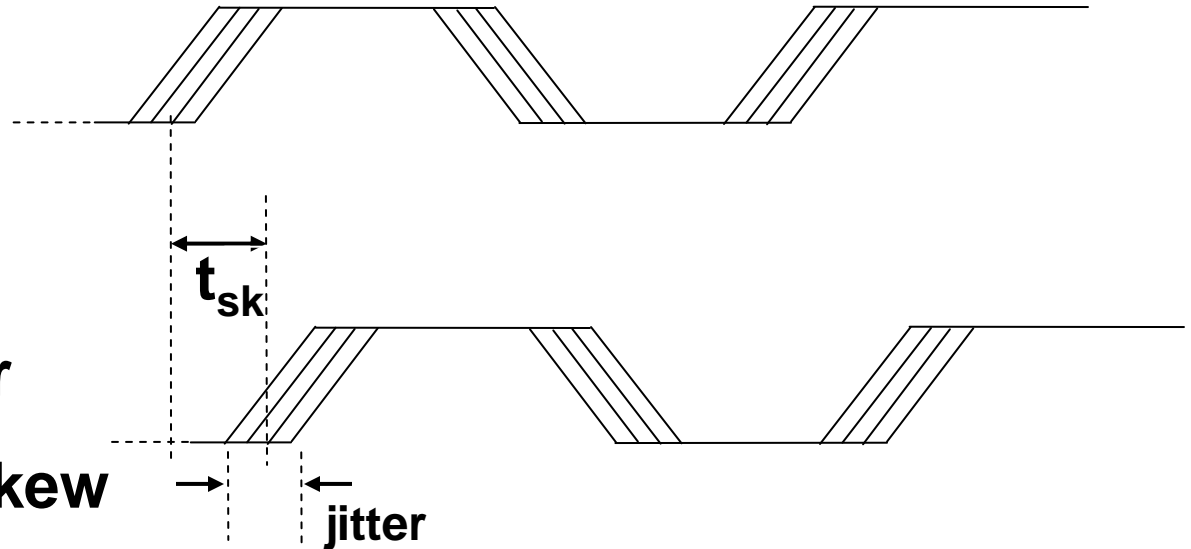
- **Generated by controlled phase modulation**
- **Reduces electromagnetic interference (EMI) to other devices**
- **Federal Communications Commission (FCC) regulates spectral content of clock sources to limit interference in nearby consumer equipment**
- **Requirement in PCIe**



- Time offset between edges of same clock at different physical locations on the board or in FPGA
- Due to different routing delays



- **Clock skew**



- **Unrelated to jitter**

- **Minimize clock skew**

- On the board

- Precise trace length matching from clock source to sinks
- Compensate by phase shifting outputs of same clock generator

- FPGA

- MMCM / DCM / PLL input clock de-skew, zero-delay buffers
- Use fast global and regional clock routing inside FPGA

- **Which applications require low phase noise / high spectral purity clock sources ?**
- **Which applications require phase modulated / spread spectrum clock sources ?**
- **What clock performance metric applies to the time domain ?**
- **What clock performance metric applies to the frequency domain ?**

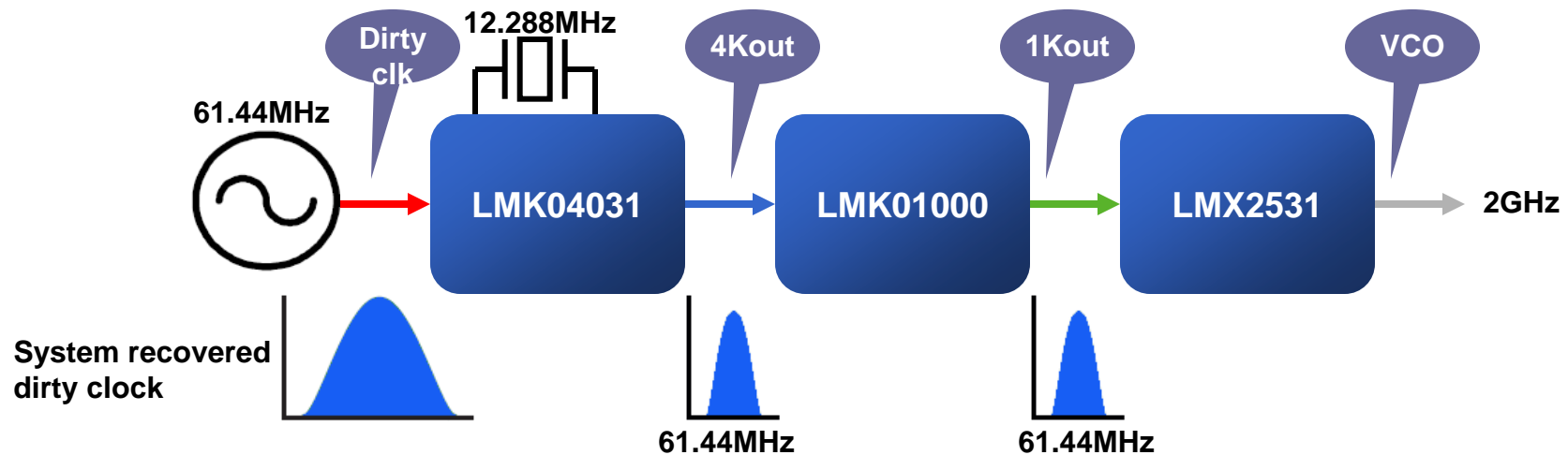
- System-Level Clocking Overview
- **High-Performance Clock Generators**
- Xilinx FPGA Clocking Resources
- Case Studies
- Demo

- **LMK01000 1.6 GHz Clock Distributor**
  - 2:8 Clock Buffer, Divider and Distributor (30 fs RMS additive)
  
- **LMK02000 Clock Conditioner**
  - Jitter Cleaning & Clock Distribution (0.2 ps RMS\* with VCXO)
  
- **LMK03000 Clock Conditioner with Integrated VCO**
  - Jitter Cleaning, Clock Generation & Distribution (0.4ps RMS\*)
  
- **LMK04000 Clock Conditioner with Dual PLL (+Crystal)**
  - Jitter Cleaning, Clock Generation & Distribution (0.15ps RMS\*)

\* Integration bandwidth of 12 kHz to 20 MHz



- **Fully Integrated Ultra-Low Noise VCO**
  - Up to 10dB better than next monolithic competitor
- **Programmable 4<sup>th</sup> order  $\Delta\Sigma$  Modulator**
  - Enhanced spurious performance
- **Freq. Range of 553 to 2790 MHz**
  - New devices up to **3132 MHz**
- **Low Supply Current (34 mA)**
  - High Output Power (+4 dBm)



- 61.44MHz dirty source recovered from system
- LMK04031's 1<sup>st</sup> PLL cleans clock with 12.288MHz crystal
- LMK04031's 2<sup>nd</sup> PLL generates clean 61.44MHz clock
- LMK01000 duplicates up to eight 61.44MHz clocks
- LMX2531LQ2080E generates low phase noise LO at 2GHz and 1GHz
- User selectable crystal or VCXO operation

## High Precision, Best in Class Jitter Performance

**CDCE62005**

*Ultra-Low Jitter, Fully Integrated*  
Clock Synthesizer / Jitter Cleaner

**CDCM61004/2/1<sup>NEW</sup>**

*Ultra-Low Jitter*  
Precision Xtal Clock Generator family  
w/ simple pin control

**CDCE72010**

*Industry's Lowest Jitter*  
Clock Generator / Jitter Cleaner  
with large fan outs

**CDCM7005**

*Industry's Lowest Jitter*  
Clock Generator / Jitter Cleaner  
with large fan outs

## Highly Flexible and Programmable Solutions

**CDCE(L)949**

*Industry's Most Flexible and Fully Programmable*  
4-PLL Clock Synthesizer

**CDCE(L)937**

*Industry's Most Flexible and Fully Programmable*  
3-PLL Clock Synthesizer

**CDCE(L)925**

*Industry's Most Flexible and Fully Programmable*  
2-PLL Clock Synthesizer

**CDCE(L)913**

*Industry's Most Flexible and Fully Programmable*  
1-PLL Clock Synthesizer

## Solving EMI with SSC Clocking

**CDCS501<sup>NEW</sup>**

*EMI Expert -*  
Spread Spectrum  
Clock Driver

**CDCS502<sup>NEW</sup>**

*EMI Expert -*  
Spread Spectrum  
Clock Driver / Multiplier  
(Xtal Input)

**CDCS503<sup>NEW</sup>**

*EMI Expert -*  
Spread Spectrum  
Clock Driver / Multiplier  
(No Xtal Input)

### Features

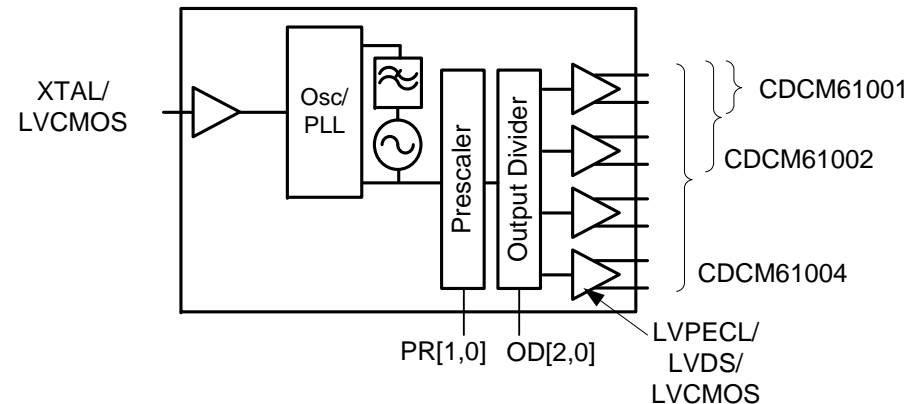
- Single ended or crystal reference input from 21.875MHz to 28.47MHz
- Fully Integrated VCO and loop filter generates various higher frequencies between 43.75-683.264 MHz
- LVCMOS output frequency up to 250MHz
- Low jitter (< 1ps RMS, 10k-20MHz), ~ 25ps, pk-pk
- Configuration changes through control pins
- Each output selectable between LVPECL, LVDS and 2-LVCMOS
- Input Crystal bypass mode: OSC\_OUT pin
- Pin-pin compatible family CDCM61004/2/1

### Applications

- Precision clock generator
- Router/Switch
- Datacom/Telecom/Networking
- Wireless Infrastructure
- Any application that needs clean clock in the supported frequency range

### Benefits

- Up to 50% cost savings to XO based solution
- One single device across multiple designs, replacing up to 4 discrete XOs
- 50% less jitter, improve BER (Bit-Error-Rate)
- Lower cost development and production
- Output interface flexibility saves additional translation logic/components on board
- Allows direct crystal tuning
- Same foot print enables the same hardware strapping for multiple designs



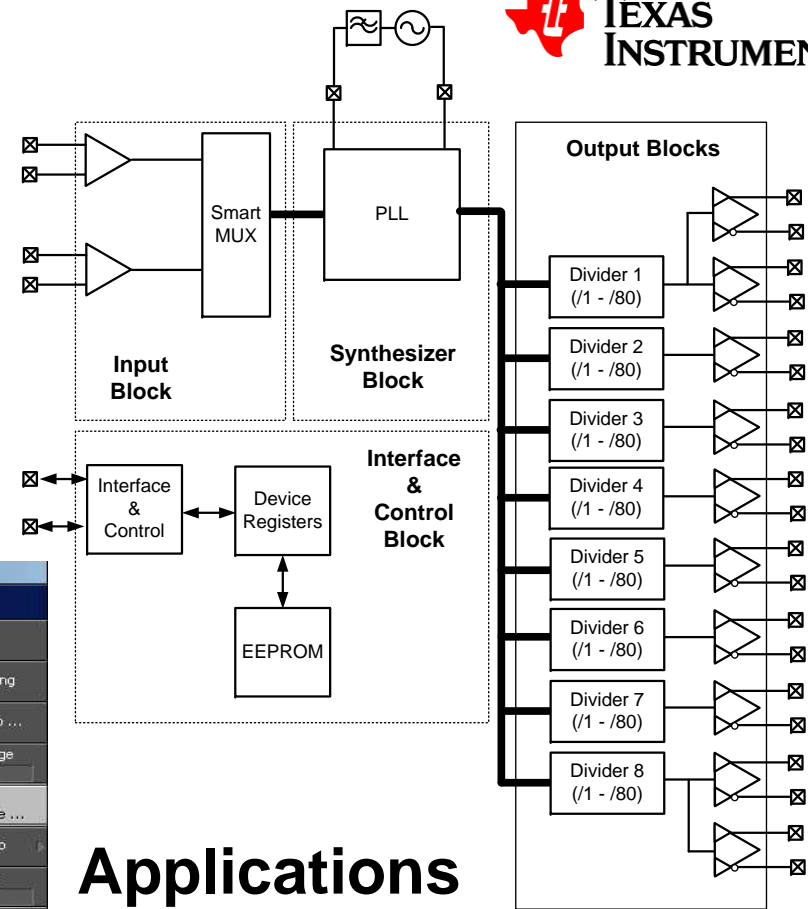
**1Ku / \$6.50/5.00/4.20**



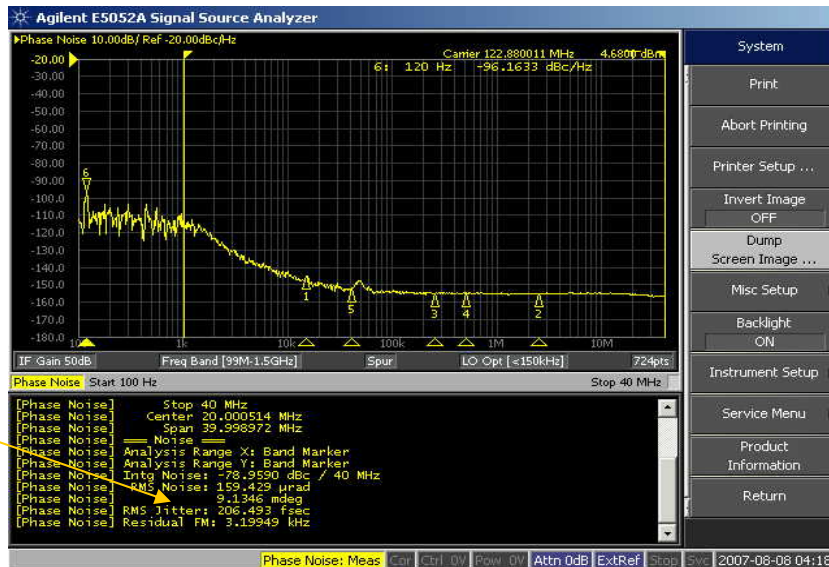


### Features

- Dual Universal Reference Inputs
  - LVPECL, LVDS, LVCMOS
  - Supports manual or automatic switchover
- Integrated Low Noise Integer-N PLL
  - Very Low Output Jitter: < 200 fs RMS
  - Residual jitter < 50 fs (distribution section)
- 10 LVPECL/LVDS and/or 20 LVCMOS Outputs
  - LVPECL up to 1500 MHz, LVDS up to 800 MHz, LVCMOS up to 250 MHz
  - Programmable skew adjust
- Host Interface: SPI
- Integrated EEPROM



$J_{RMS} = 206 \text{ fs}$   
1KHz-40MHz



### Applications

- Wireless Systems
- High Performance ADC/DAC Clocking
- High Speed Communication Links

## Features

- Crystal input from 8MHz to 32MHz
- Selectable multiplier rates of 1x and 4x so that generate output frequency from 8MHz to 110MHz
- Selectable Spread-Spectrum Modulation of  $\pm 0.5\%$ ,  $\pm 1.0\%$ , and  $\pm 2.0\%$
- 8 pin TSSOP package
- Single 3.3V power supply, wide temperature range -40 , 85

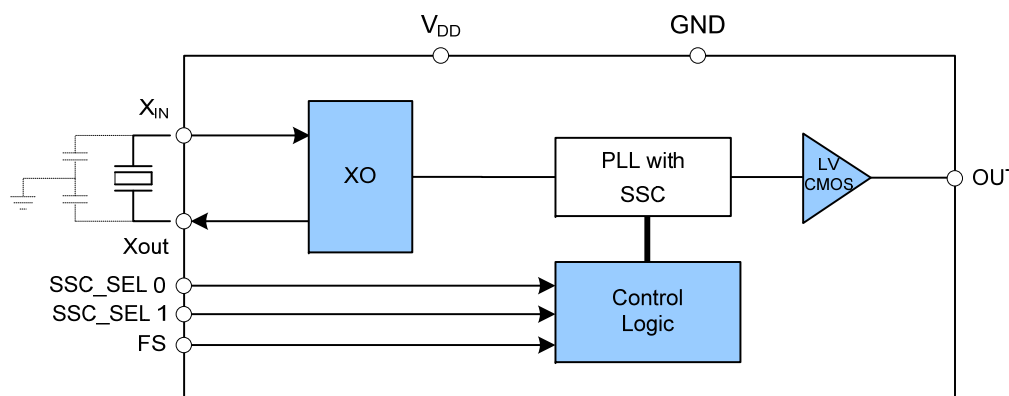
## Applications

- XO replacement with EMI reduction need:
- Digital Audio/Video Entertainment
  - Flat Panel TV; Set-top Boxes; Blu-Ray DVDR
- PCs, Printers
- Communications access point/gateway/networking card
- Industrial

**1Ku / \$0.95**

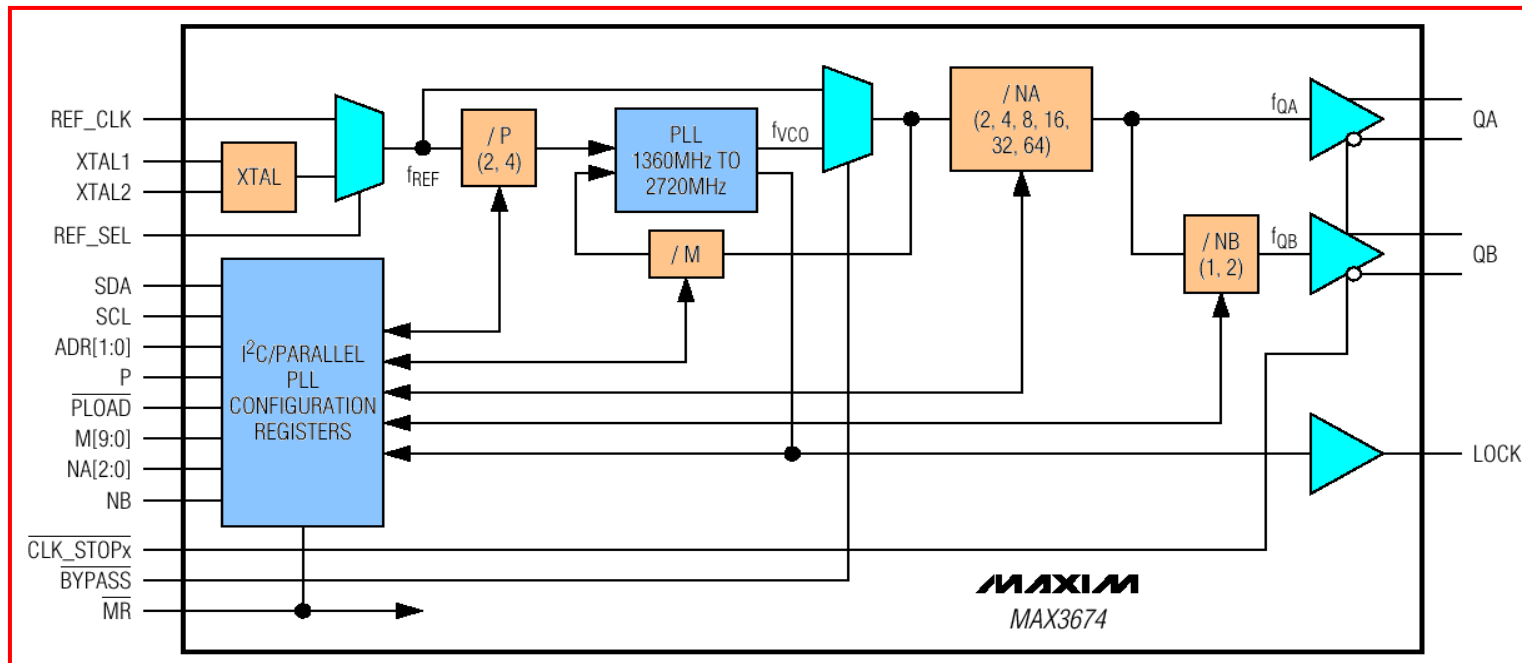
## Benefits

- Replacing more costly crystal oscillators
- Wider output frequency range enables one device across multiple designs
- Reduce EMI thru selectable amount of SSC modulation up to 10dB
- Low board space consumption
- Simple power supply scheme; Applicable to wider applications with improved reliability



X <sub>IN</sub>	1	CDCS502	8	X <sub>OUT</sub>
SSC_SEL 0	2		7	VDD
SSC_SEL 1	3		6	OUT
GND	4		5	FS

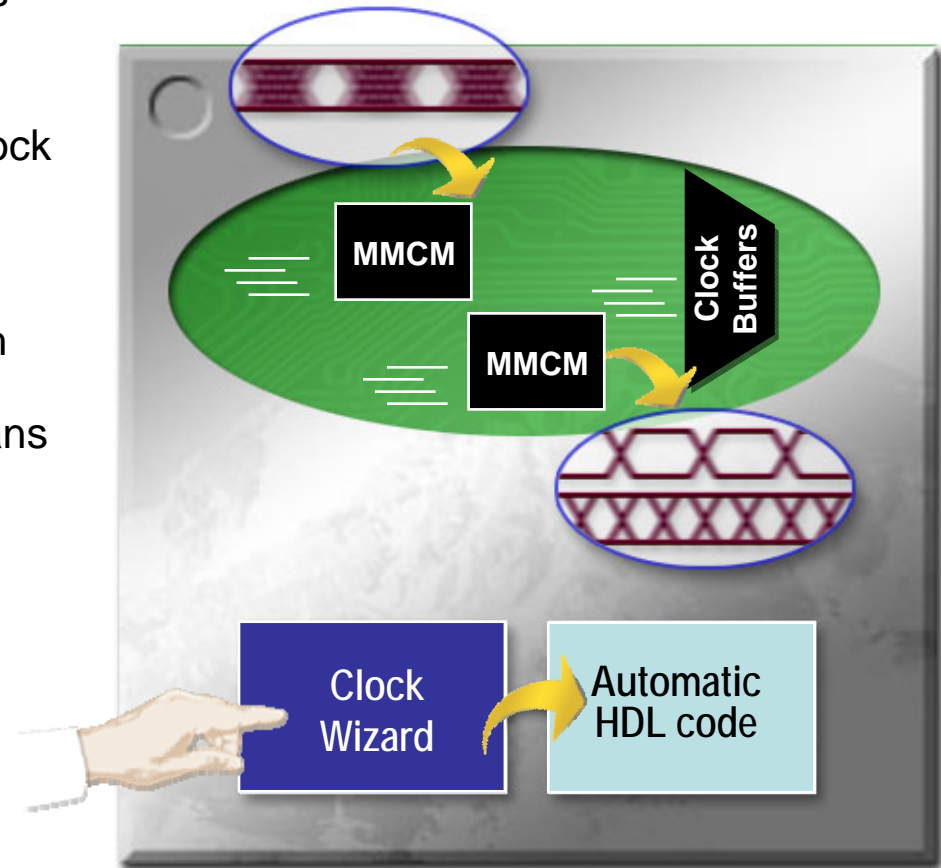
- **Spartan-6 GTP reference clock source**
- **Meets or exceeds the specifications of Xilinx recommended oscillators**
  - Dual programmable differential LVPECL outputs
  - Output frequency range of 21.25MHz to 1360MHz
  - Crystal input frequency range of 15MHz to 20MHz
  - Total period jitter of 18ps (typical)



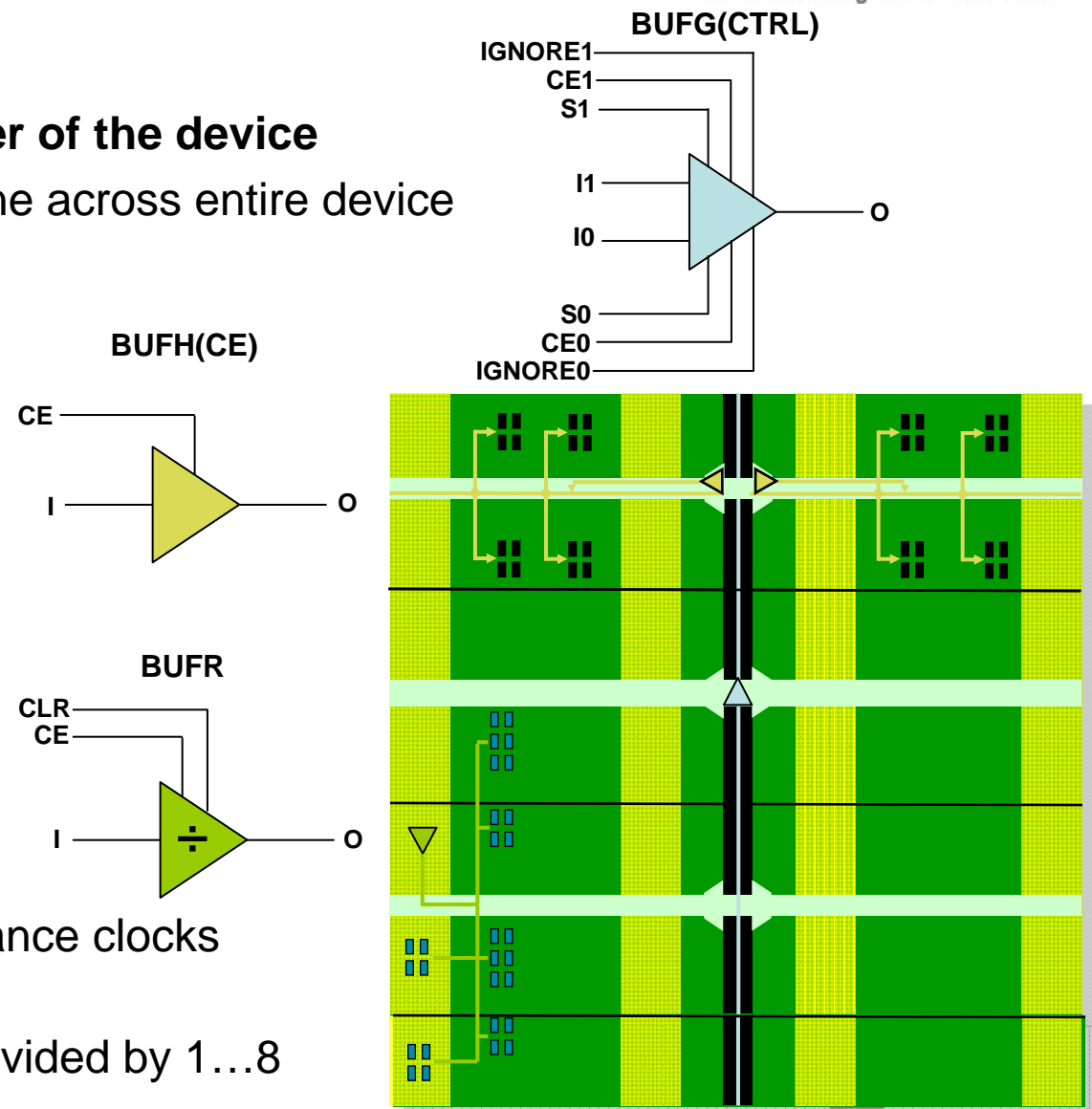
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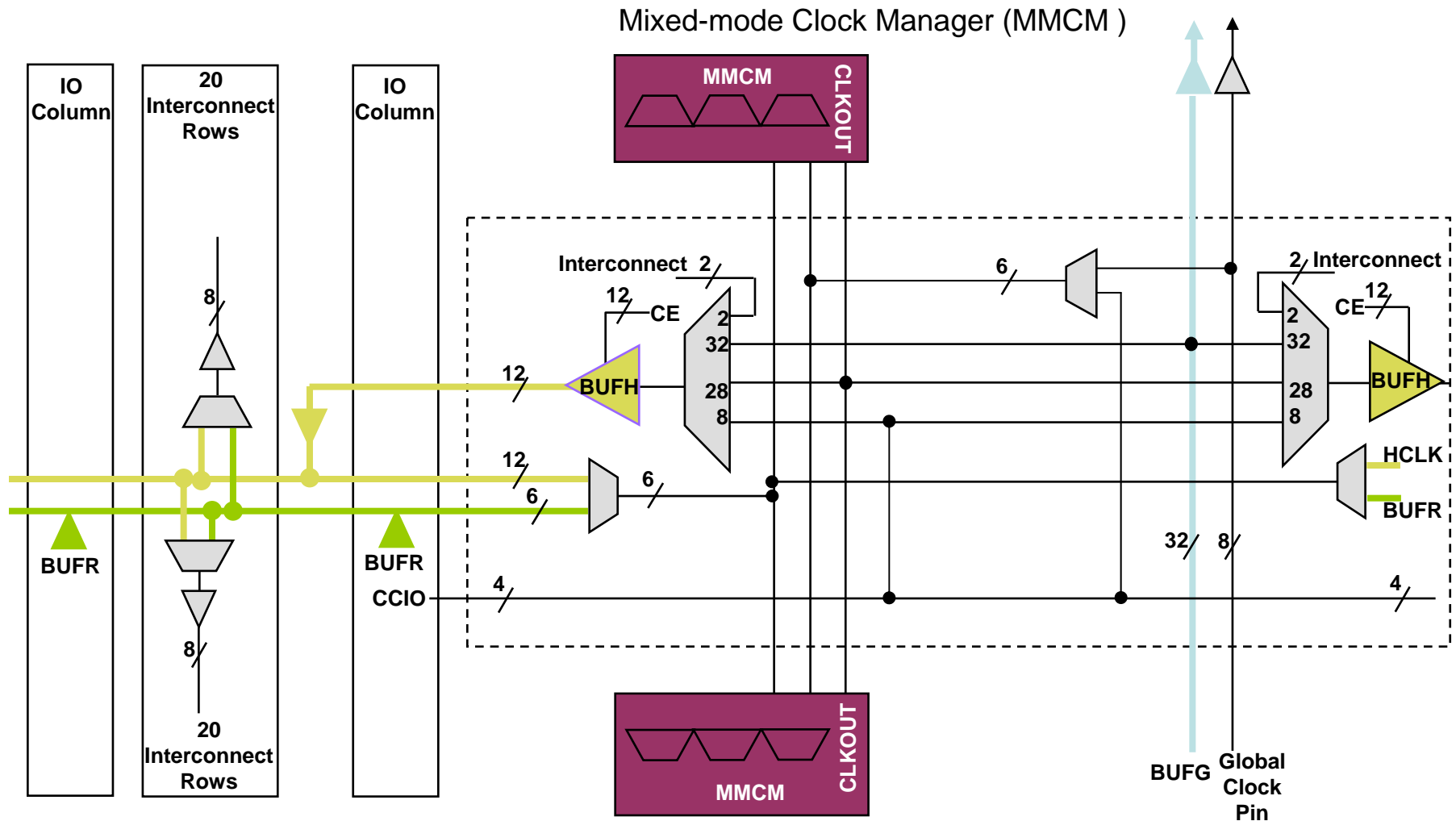


- **Low-skew clock distribution**
  - Combination of paths for driving clock signals to and from different locations
  
- **Clock buffers**
  - High fanout buffers for connecting clock signals to various routing resources
  
- **Clock regions**
  - Device divided into clock regions with dedicated resources
  - Each region is 40 CLBs high and spans half the device
  
- **Clock management tile (CMT)**
  - Two PLL-based Mixed-Mode Clock Managers in each CMT
  - Up to nine CMTs per device
  - Performs frequency synthesis, clock de-skew and jitter-filtering
  
- **Easy-to-use software**
  - Fast and simple access to the circuitry



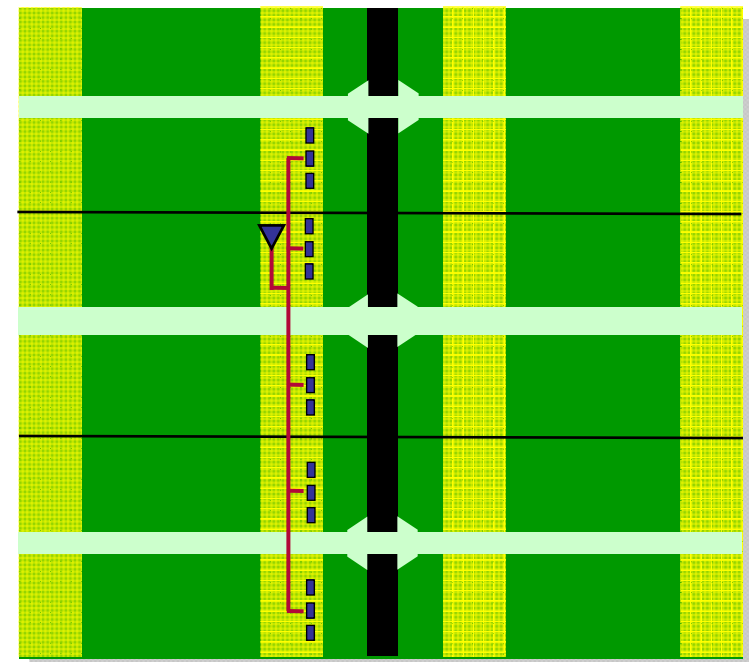
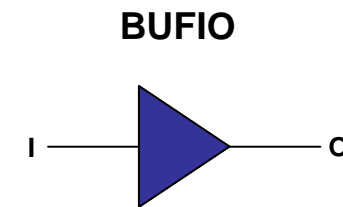
- **All 32 BUFGs reside in center of the device**
  - Can drive global clock spine across entire device
  
- **Twelve BUFGs per clock region**
  - Up to eighteen clock regions per device
  - Power saving by turning off, or gating, clocks to specific regions
  
- **Up to 8 BUFRs per clock region**
  - For medium-high performance clocks used within 1-3 regions
  - BUFR frequency can be divided by 1...8



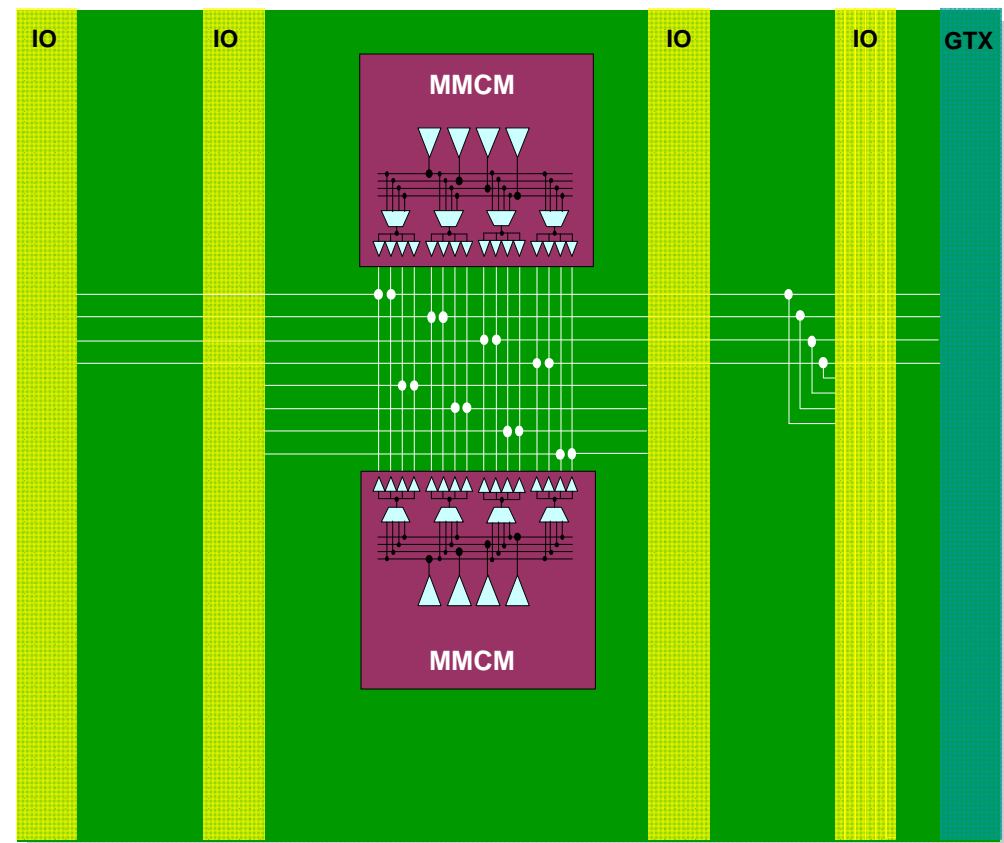


BUFH is the access point for global clocks to enter a clock region

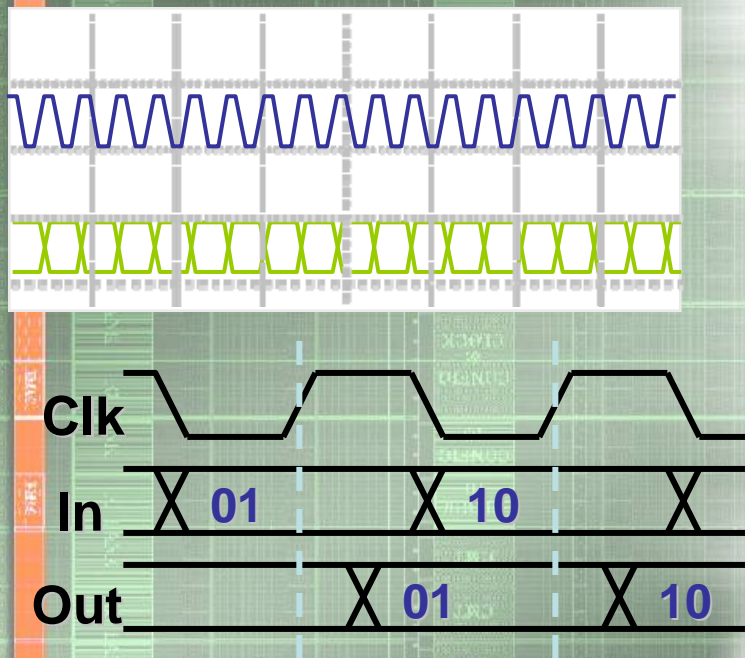
- **Two single-region BUFIOs and two multi-region BUFIOs in each region**
- **Driven by:**
  - Clock Capable Inputs in the same clock region
  - MMCM outputs via High-Performance Paths
- **Can drive:**
  - IO Logic in the same and adjacent regions
  - BUFIO can drive logic resources only in the same IO column
- **Intended for clocking high speed IO logic**



- **Four Performance Paths driving each inner/outer L/R IO column**
- **Driven by MMCM outputs O0-O3**
- **Can drive BUFIO, BUFR**
- **Powered by regulated supply within each MMCM**
  - Isolated from noise on Vccint
  - Cleanest path from MMCM to IO columns
  - Lower jitter than any other routing
- **Best performance for clock forwarding through OSERDES**



Performance Paths enable fast IO interfaces



- **Systems usually require multiple clock frequencies from the same source**
  - Minimizing the number of oscillators lowers system cost
- **External clock sources can often be noisy**
  - Filtering jitter cleans up clocks widening the data valid window
- **Many circuits need to be clocked at the same time to ensure correct operation**
  - De-skewing and aligning clocks eliminates hold-time issues and race conditions

- Phase / frequency detector compares CLKIN with CLKFB

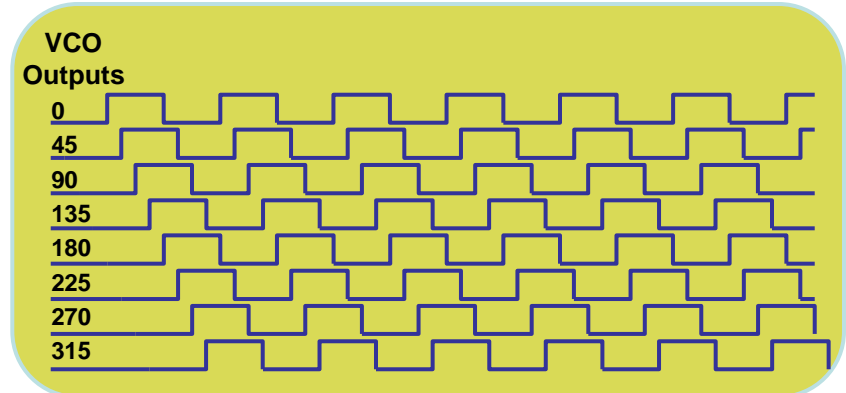
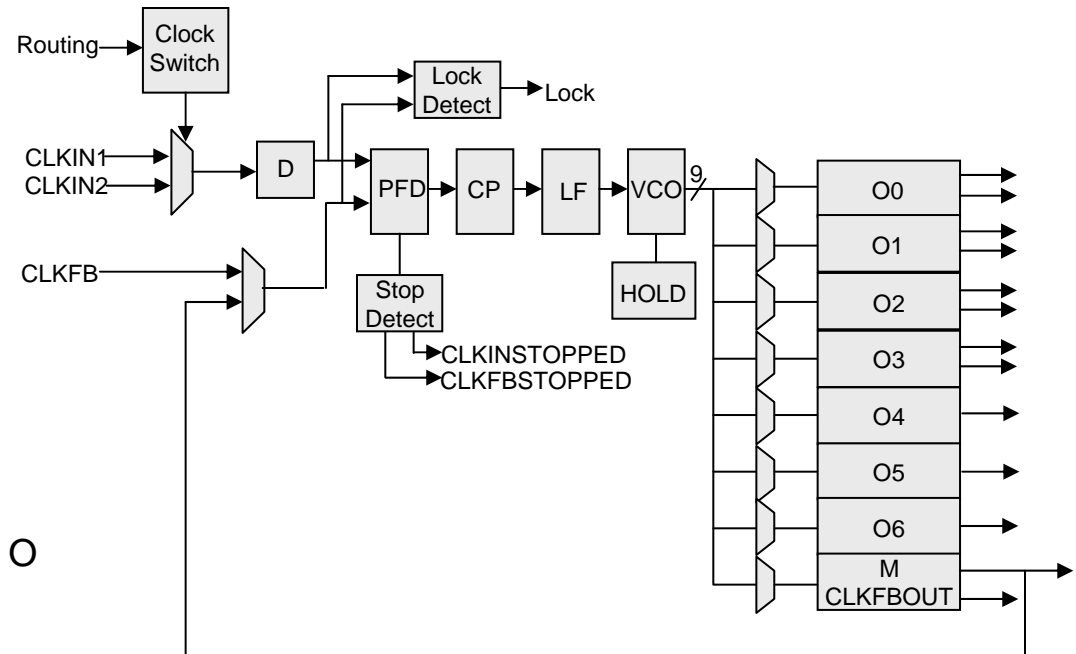
- Up to 550 MHz inputs
- Adjusts charge pump output voltage
- Charge pump controls the VCO frequency (up to 1.6 GHz)

- Versatile frequency synthesis

- $F_{out} = F_{in} * M / (D * O)$
- One M and one D value per MMCM
- Each MMCM output can have its own O value
- M: 1...64; D: 1...80; O: 1...128

- Two methods of shifting phase

- Static Phase Shift using time-shifted VCO outputs
- Dynamic Phase Shift using the PS port to change the phase on the fly in increments of 1/56 of VCO period

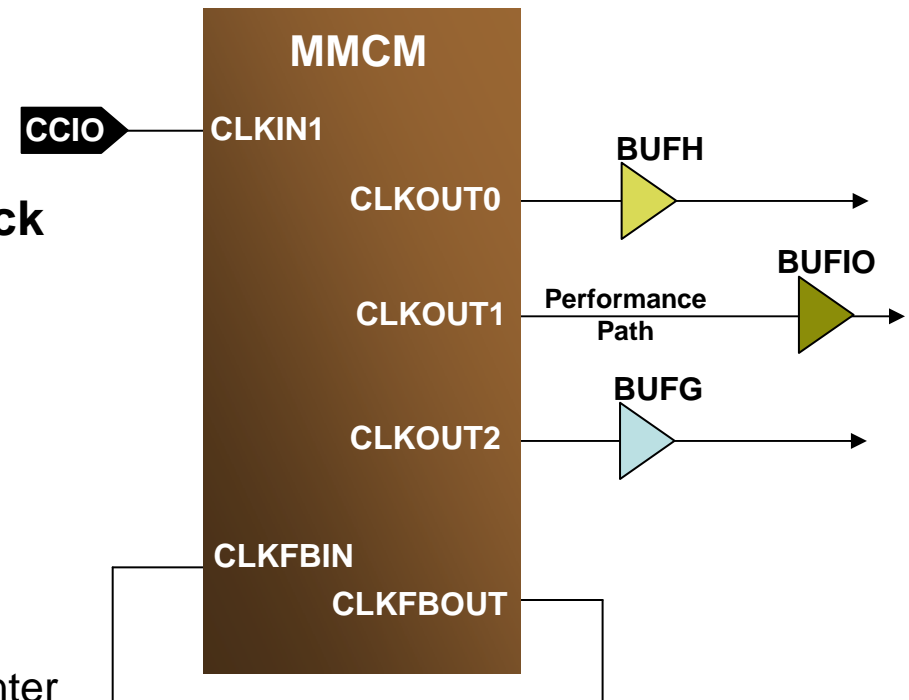


## Requirement:

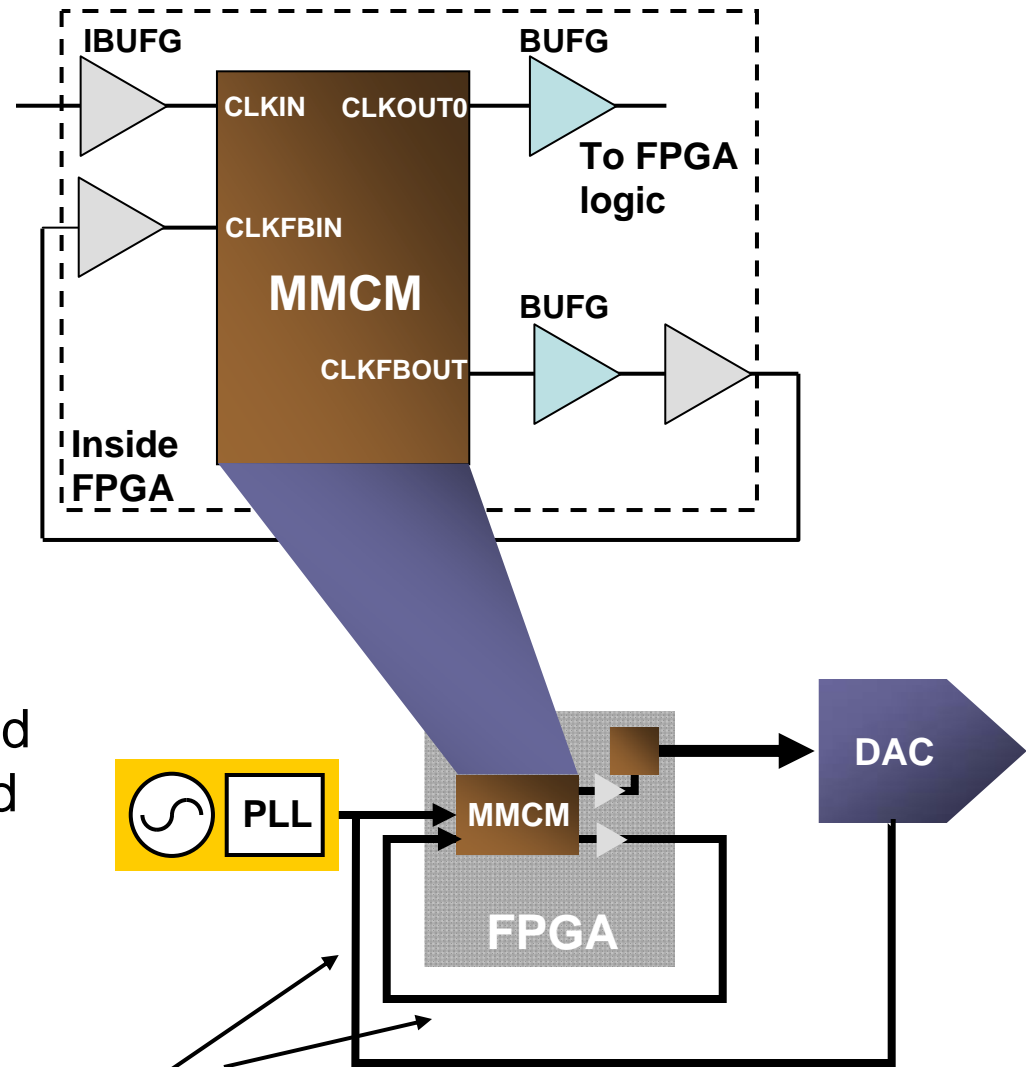
- **33.3 MHz external oscillator controls:**
  - 533 MHz data captured by IO logic
  - Large amount of logic at 66 MHz
  - Small design at 54 MHz
- **Phase relationship between input clock and output clock is irrelevant**

## Solution:

- **MMCM values**
  - M=16, D=1, O0=9.875, O1=1, O2=8
- **Generates:**
  - 54 MHz on clkout0
    - O0 set to 9.875 using fractional counter
  - 533 MHz on clkout1
    - Drives BUFIO via performance path
  - 66 MHz on clkout2
    - Drives BUFG for general distribution



- **Single clock drives multiple external components**
- **FPGA aligns clocks at the board level to minimize skew**
- **Feedback signal also drives off- chip**
  - Board trace length matches trace length to external components
  - Clock edges are thus aligned at the input of the FPGA and the input of the external component

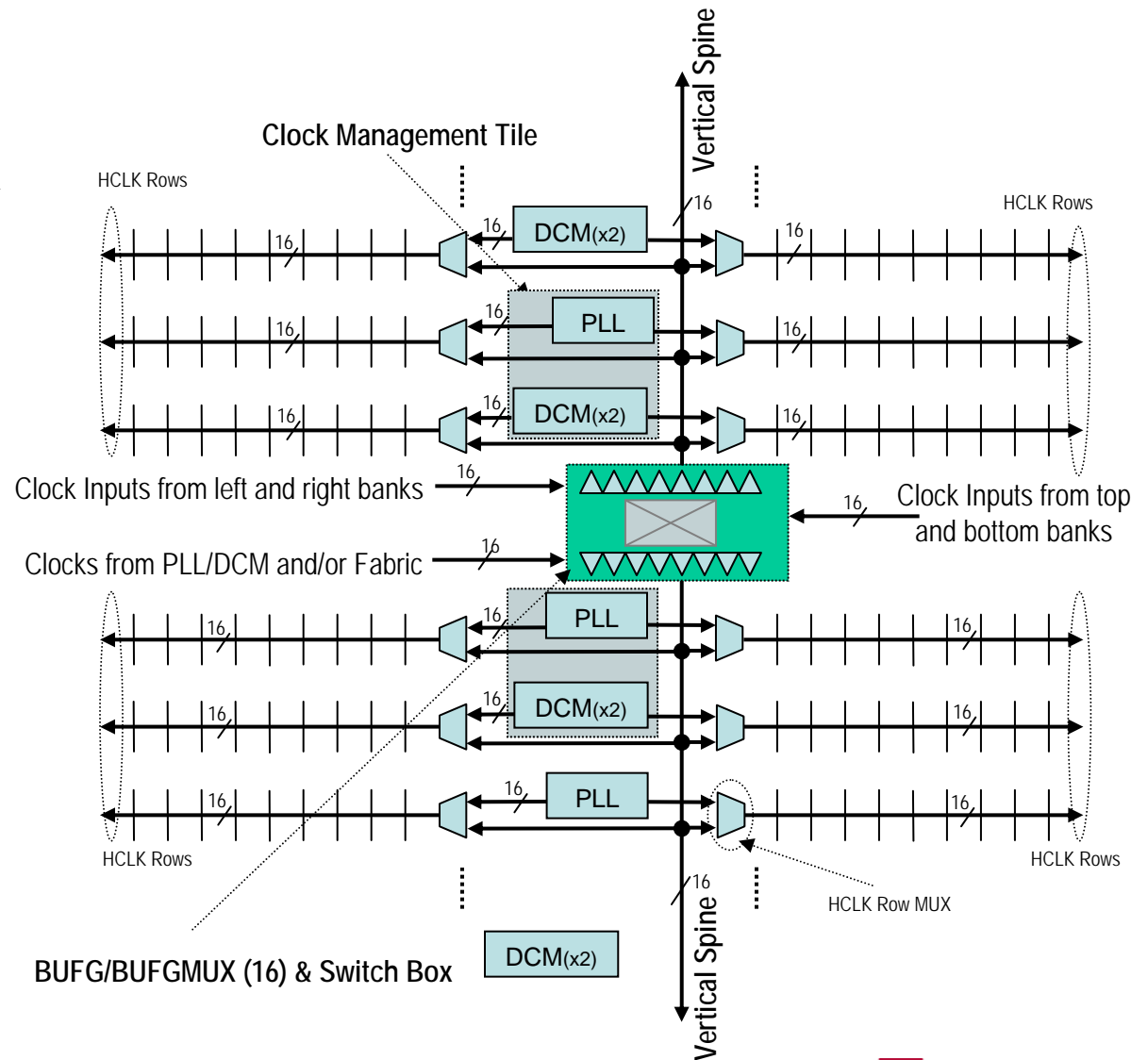


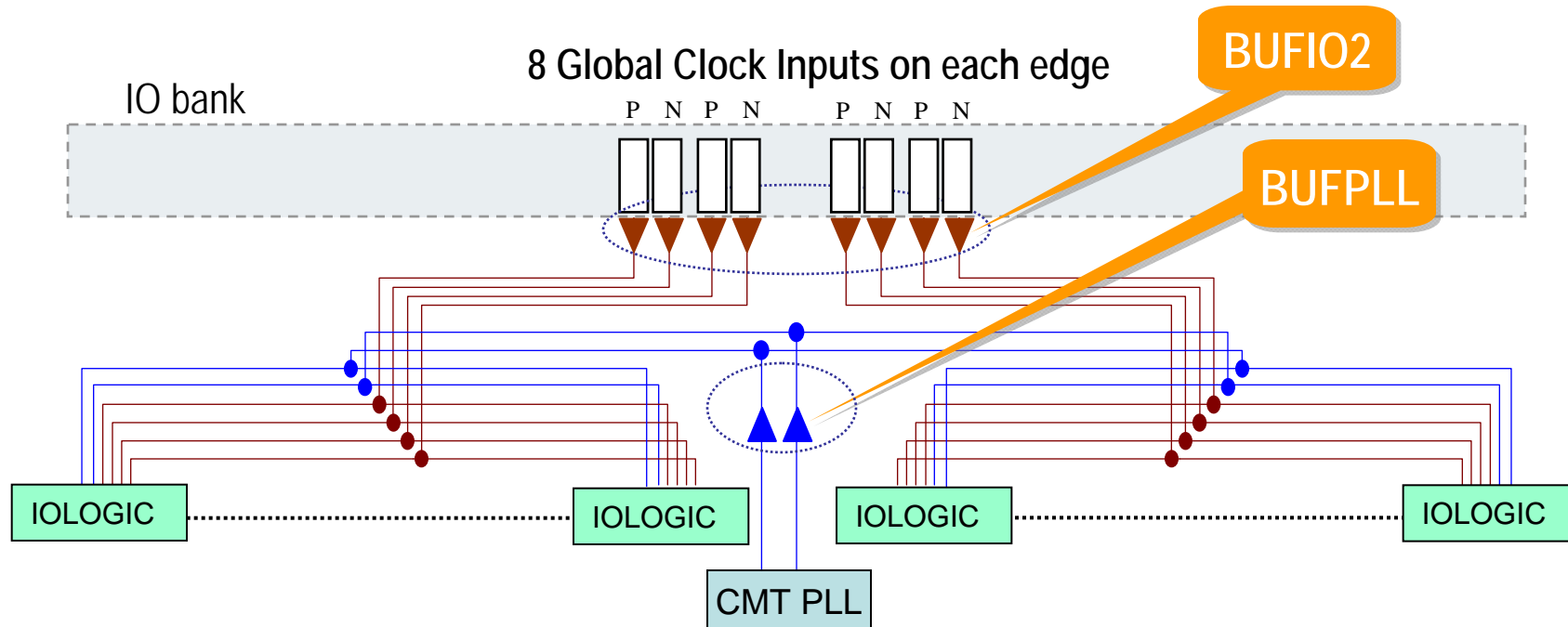
Equal length traces on the board

- **Two Types of Clock Networks:**
  - **Enhanced global clock network**
    - Up to 16 global clocks in each device
    - Maximum frequency: 375 MHz
  - **Dedicated IO clock network**
    - Ultra-fast speed: up to 1 GHz
    - Four IO clocks per half bank
    - Two IO clocks spanning entire bank
- **Virtex<sup>®</sup>-5-Like Clock Management Tile (CMT)**
  - One to six total CMTs
  - Two feature-enhanced DCMs per CMT
    - Derived from the successful Spartan-3A DCM
  - Plus one PLL per CMT
    - Derived from the successful Virtex-5 PLL

***Major architectural changes over previous generation***

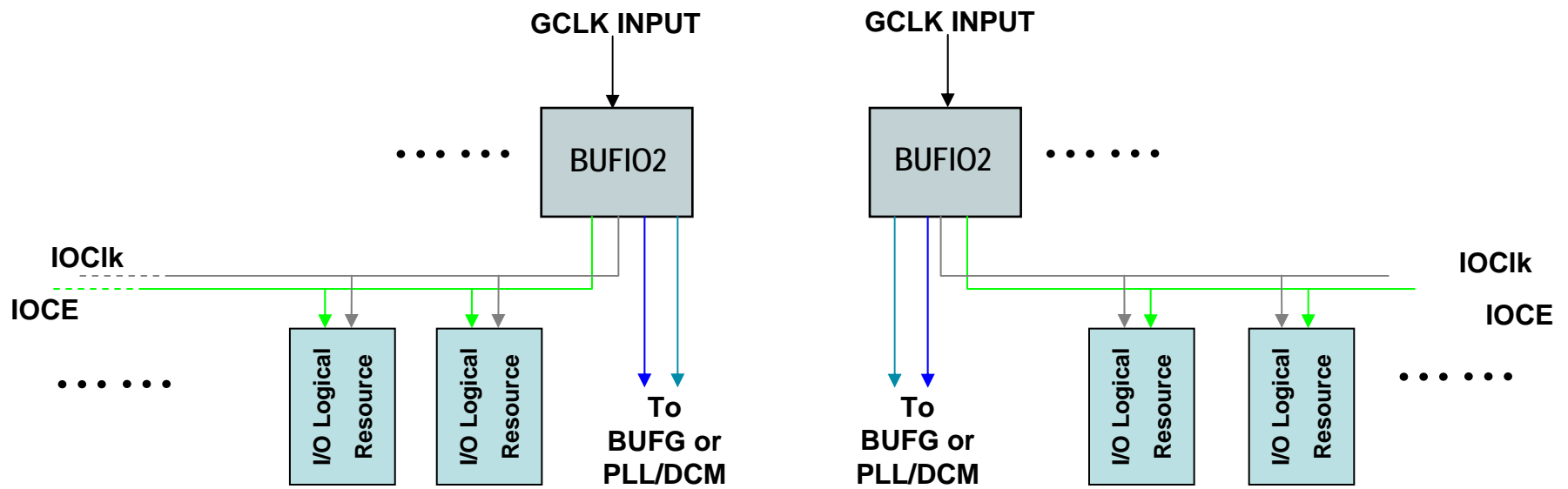
- All 16 BUFGs located in center
- Vertical spines connect selectively to horizontal HCLK rows
- All regional fabric components are driven by BUFH



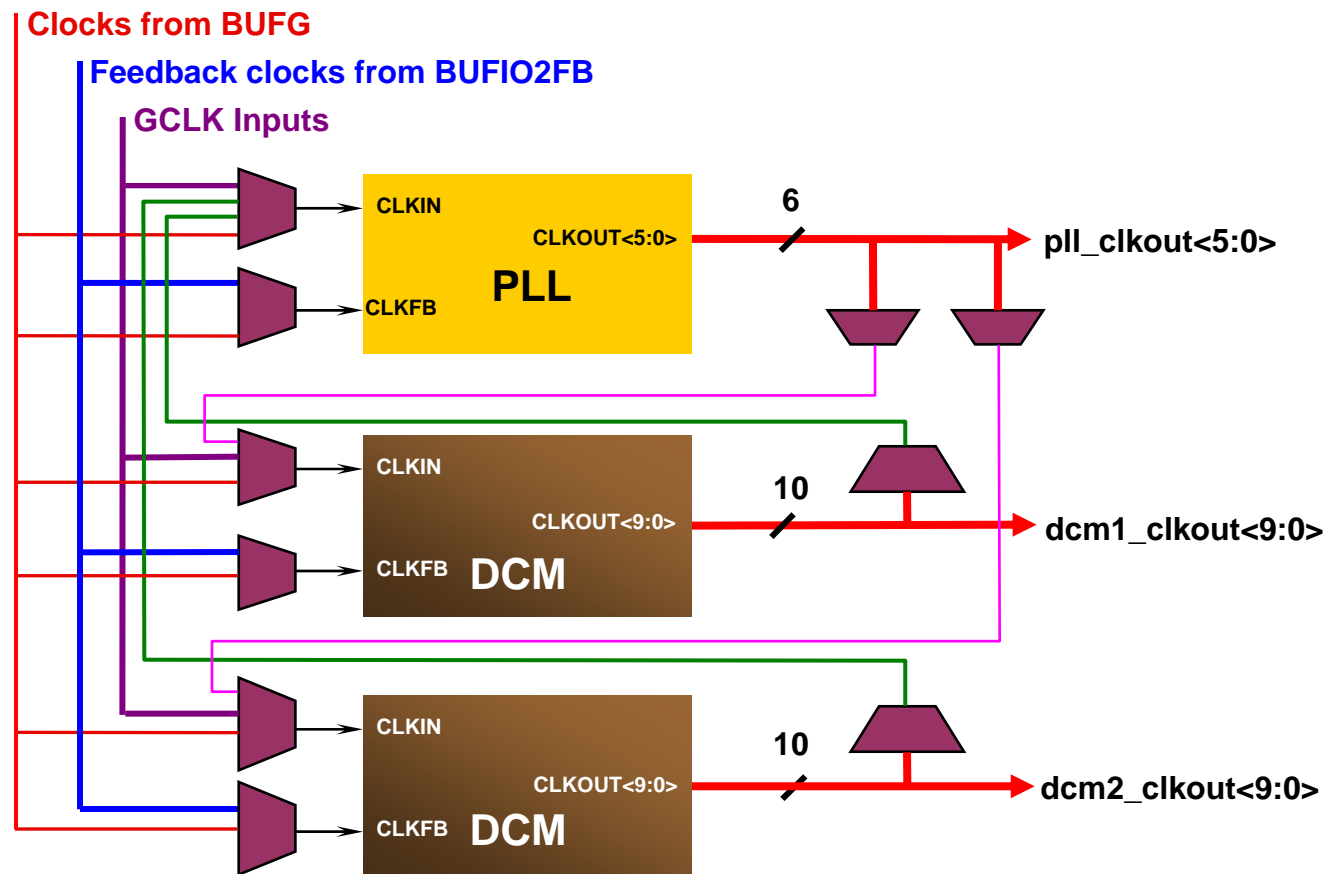


- **Special clock network dedicated for I/O logical resources**
  - Independent of global clock resources
  - Super-fast speed up to 1 GHz
- **Dedicated clock drivers, driven by specific pins**
  - BUFIO2: for clock inputs
  - BUFPLL: for CMT PLL

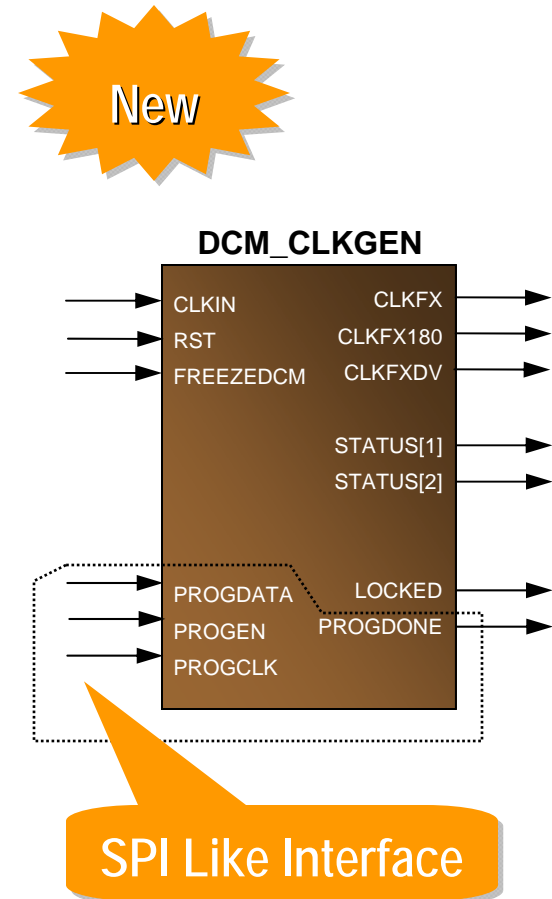
- **BUFIO2 routes an input clock through dedicated paths to**
  - IOCLK network
  - BUFG and then GCLK network
  - PLL/DCM directly



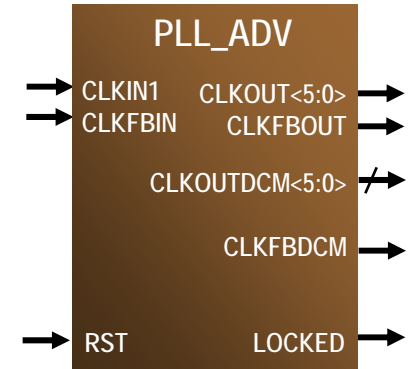
- Up to six CMTs per device
- Each CMT = one PLL + two DCMs



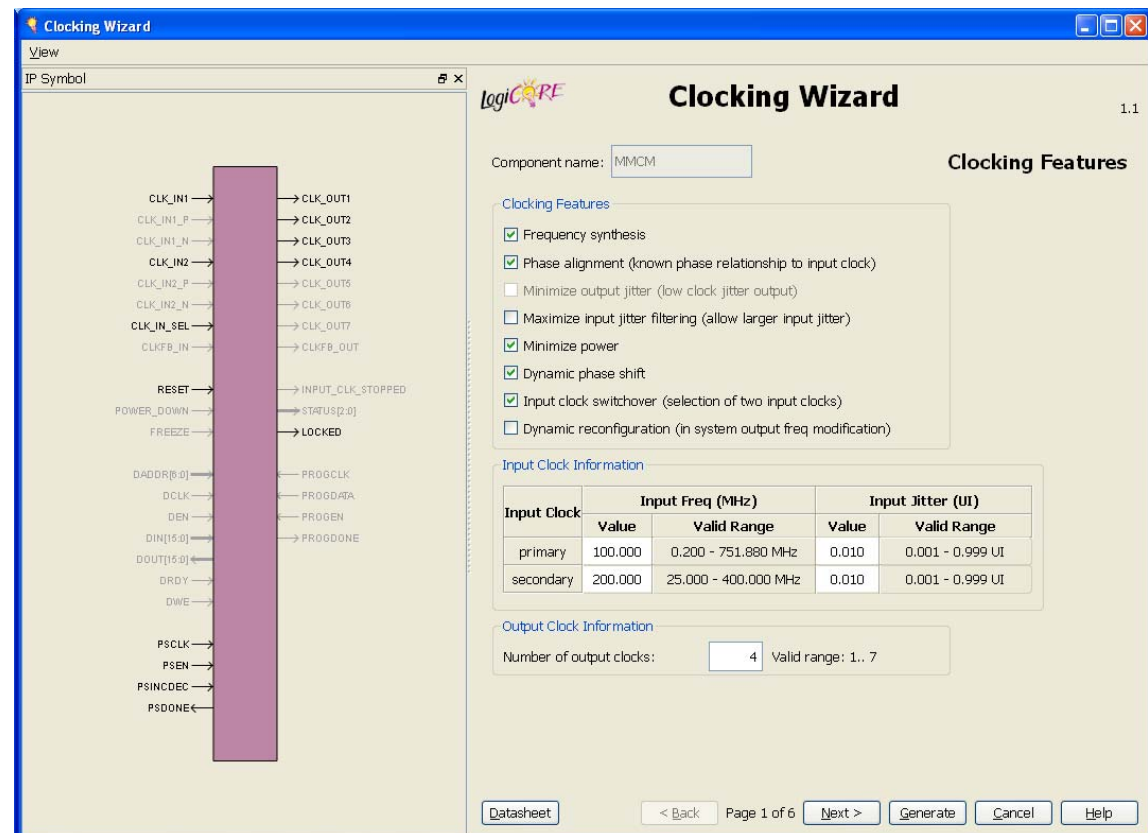
- **Provides advanced clock management features**
  - Dynamic Frequency Synthesis
    - Change M/D on-the-fly through an SPI-like interface
    - M: 2 to 255
    - D: 1 to 255
  - Free Running Oscillator
    - An initial CLKIN toggling is required
    - Freeze DCM once LOCK is achieved
    - CLKIN can be simply switched away
  - Can generate Spread Spectrum Clocks
  
- **Implements only advanced DFS functions**
  - DLL is turned off
  - No phase shift is available
  - No phase alignment is available



- **CLKIN from 19 MHz – 500 MHz**
  - Internal VCO up to 1GHz for more flexible frequency synthesis
- **Synthesize  $F_{out} = F_{in} * M / (D * O)$** 
  - M: 1-64, D: 1-52, O: 1-128
- **Additional PLL\_ADV features**
  - Cascade clocks to and from DCMs
  - Can port legacy Virtex-5 designs to Spartan-6

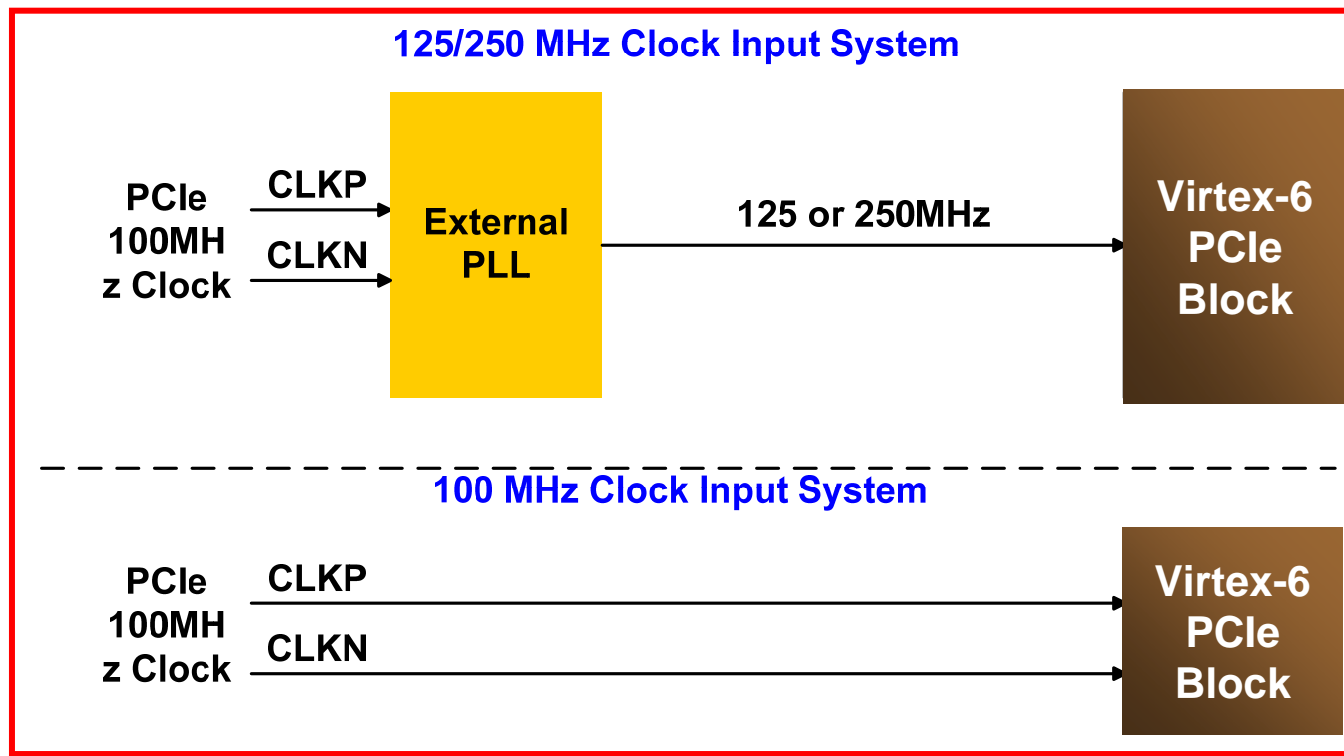


- **Core Generator-based Clocking Wizard**
  - Same new wizard for Virtex-6 & Spartan-6
  
- **Fully customizable**
  - Clear, concise summary of resource utilization
  
- **Performs all the calculations on the user's behalf**

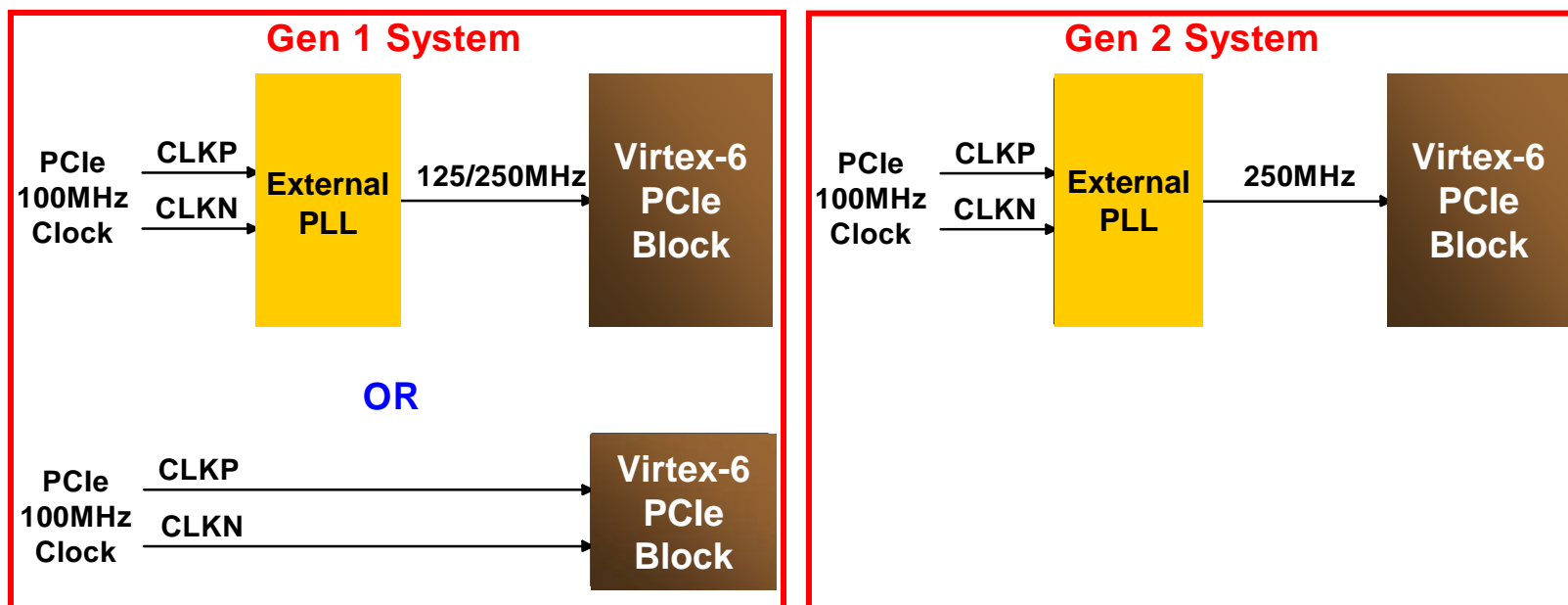


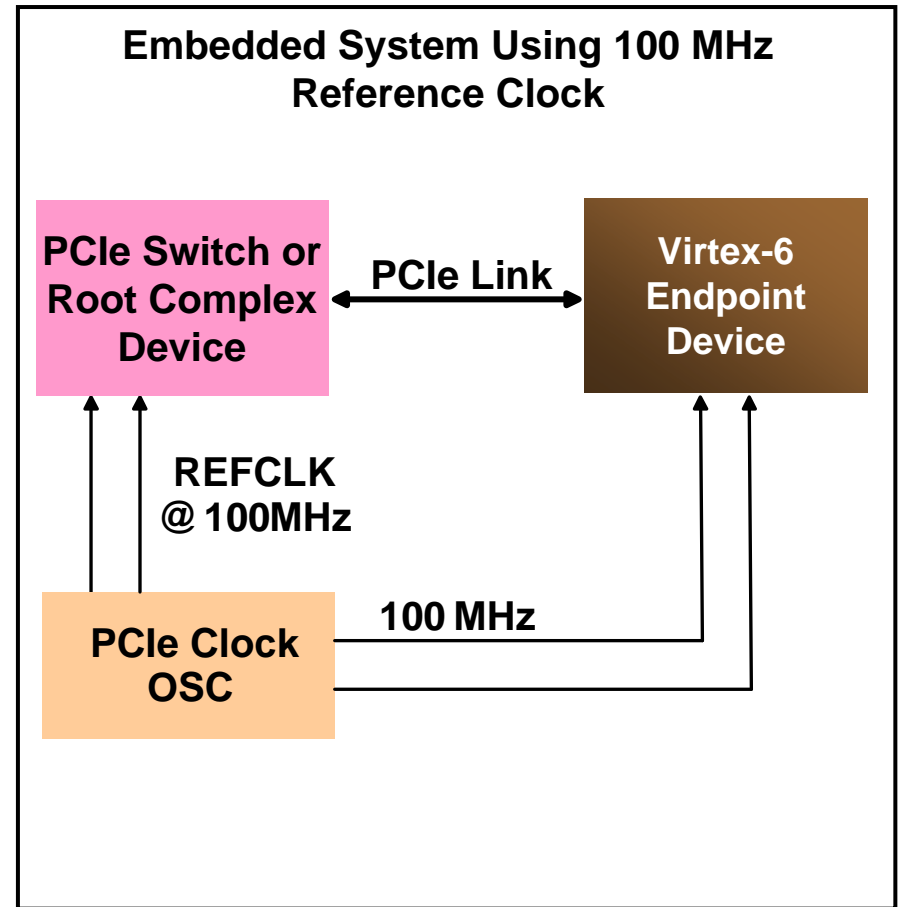
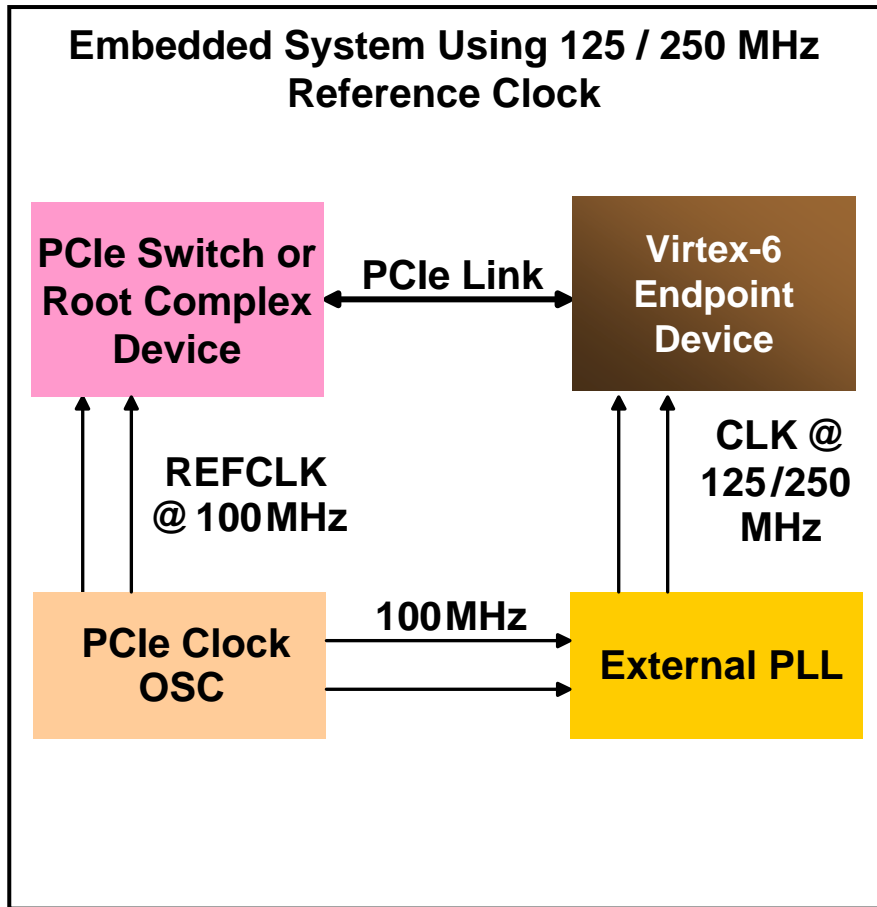
- System-Level Clocking Overview
- High-Performance Clock Generators
- Xilinx FPGA Clocking Resources
- **High-Speed Serial IO Clocking**
- Case Studies
- Demo

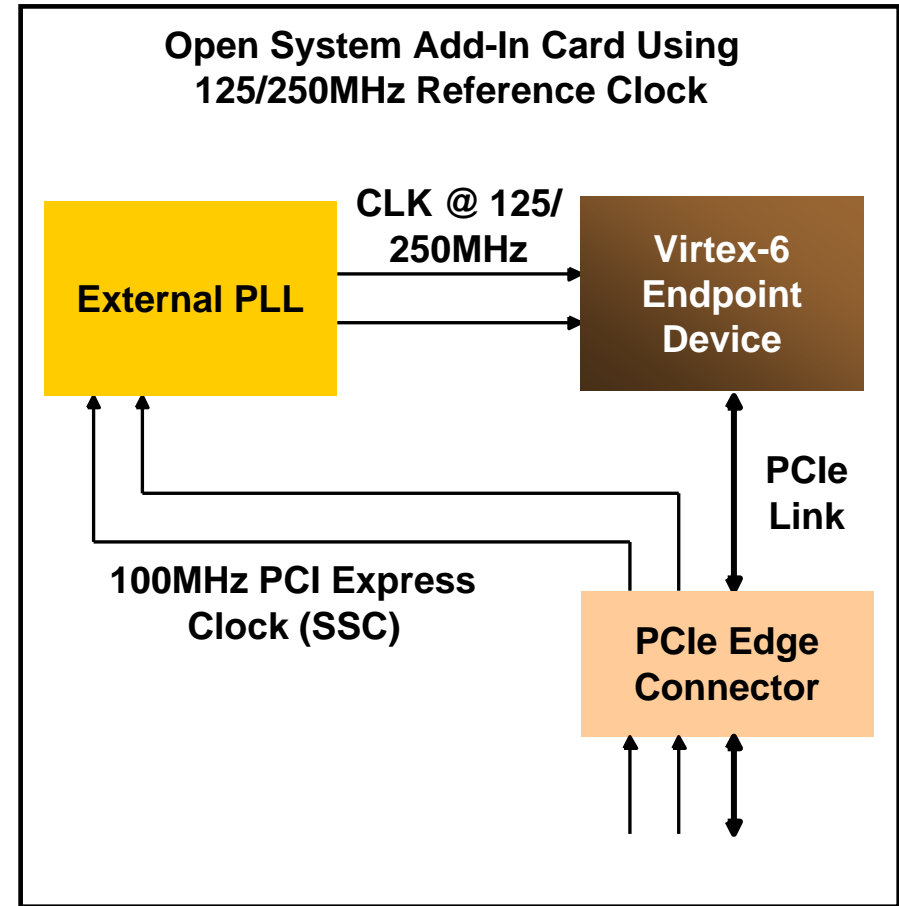
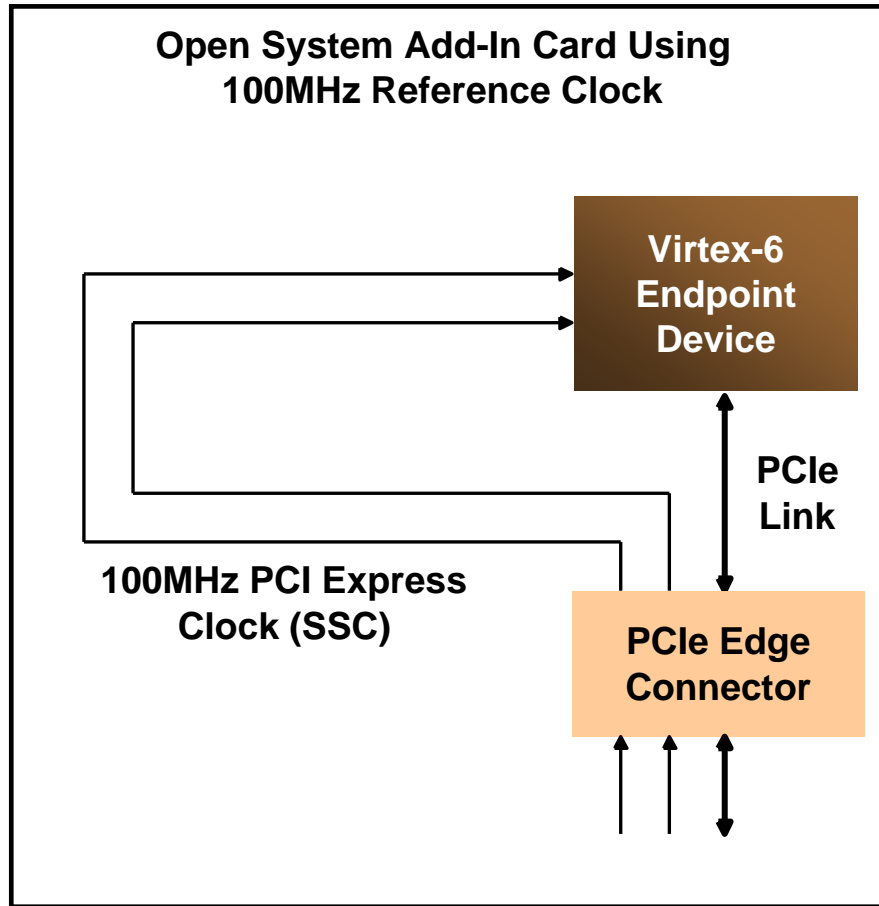
- The Integrated Endpoint Block input system clock signal is called ***sys\_clk***. The core requires a 100MHz, 125 MHz or 250MHz clock input
  - The clock frequency used must match the clock frequency selection in the CORE Generator GUI
  - In a typical PCI Express solution, the PCI Express reference clock is a Spread Spectrum Clock (SSC), provided at 100MHz



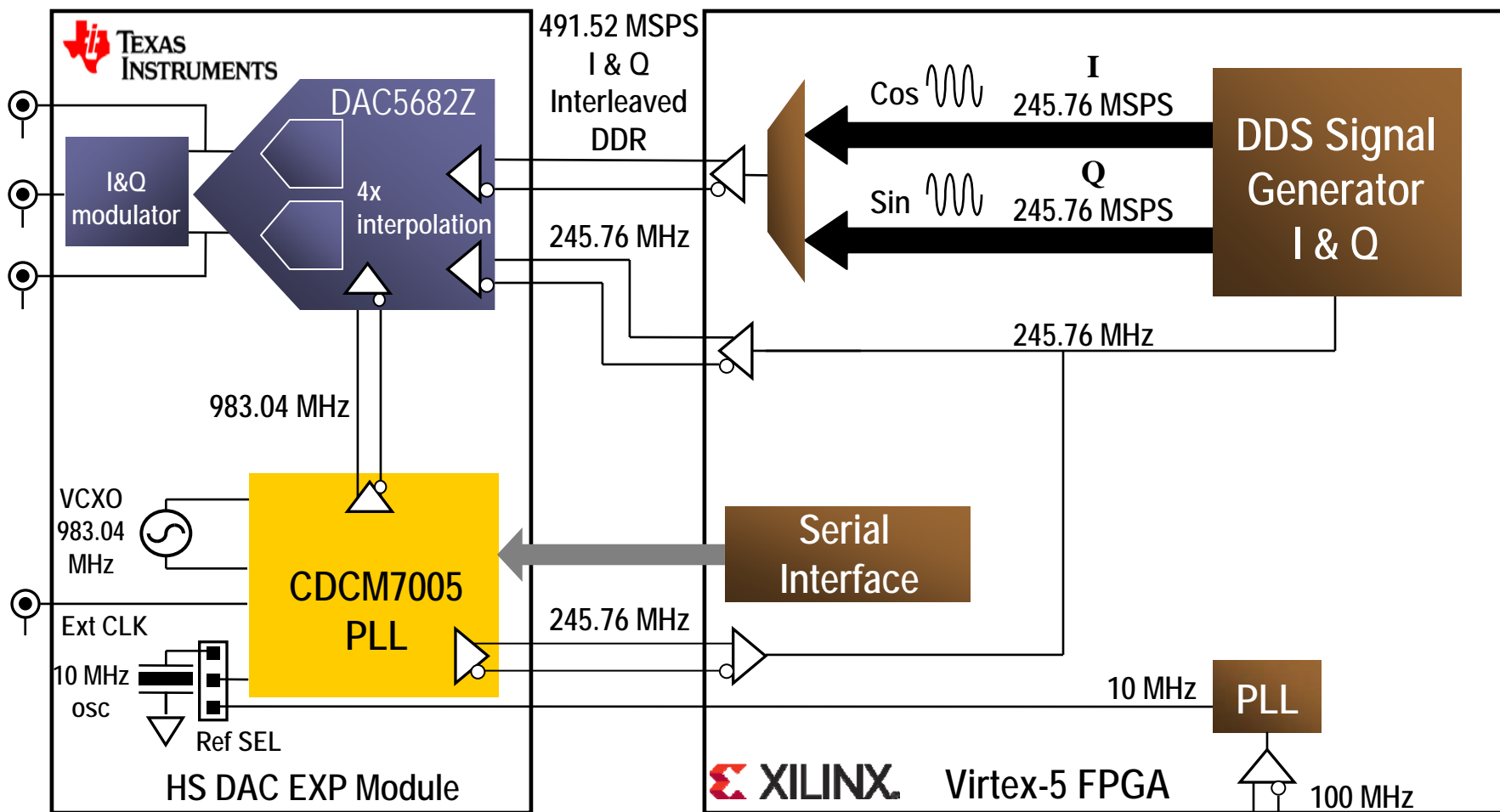
- The Virtex-6 PCIe block operated at Gen 2 data rate will require a 250MHz input reference clock
  - This restriction may be removed in a future version of this core
  
- The Virtex-6 PCIe block operated at Gen 1 data rate can use a 100, 125, or 250MHz input reference clock





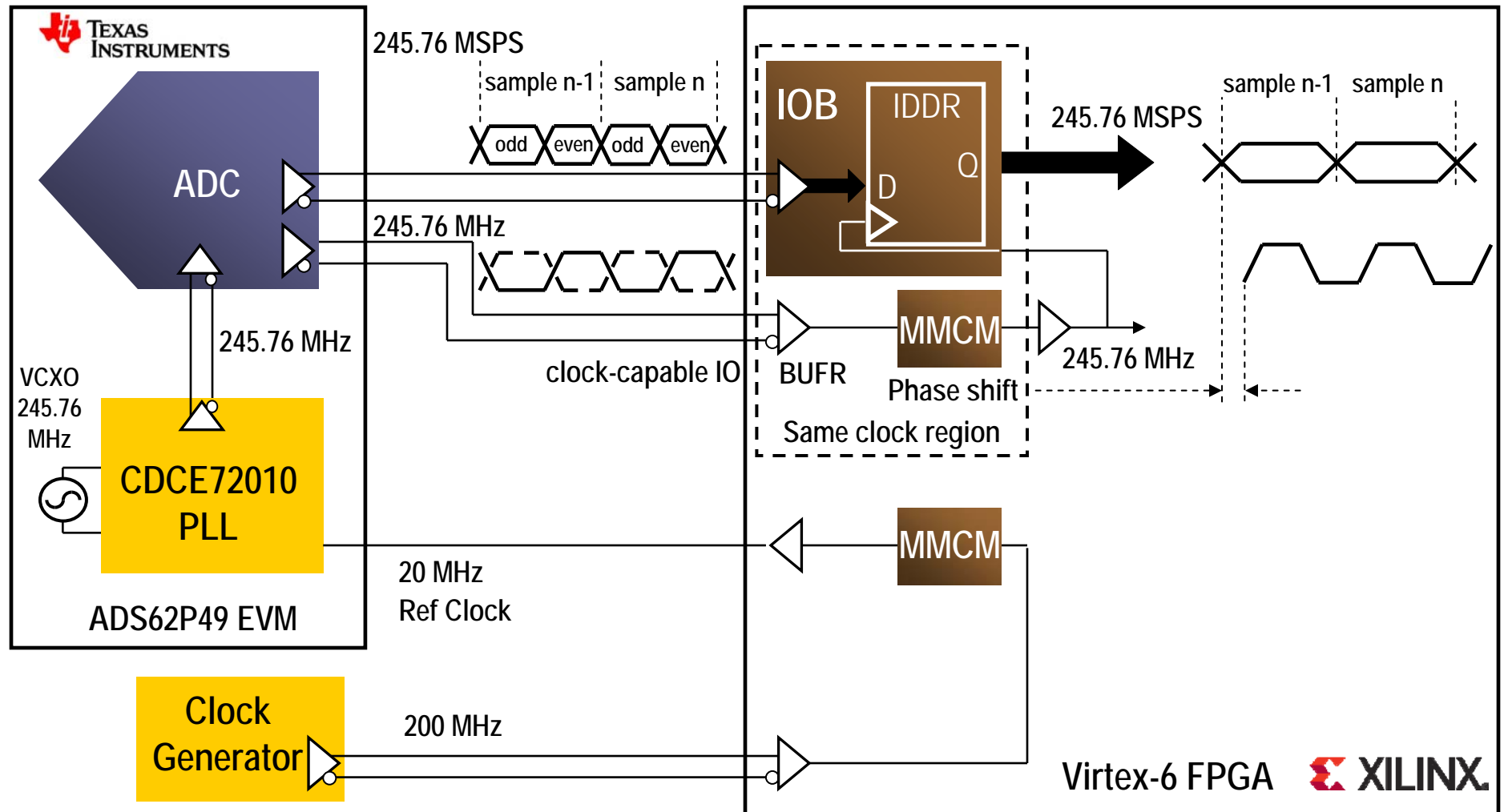


- System-Level Clocking Overview
- High-Performance Clock Generators
- Xilinx FPGA Clocking Resources
- **Case Studies**
- Demo

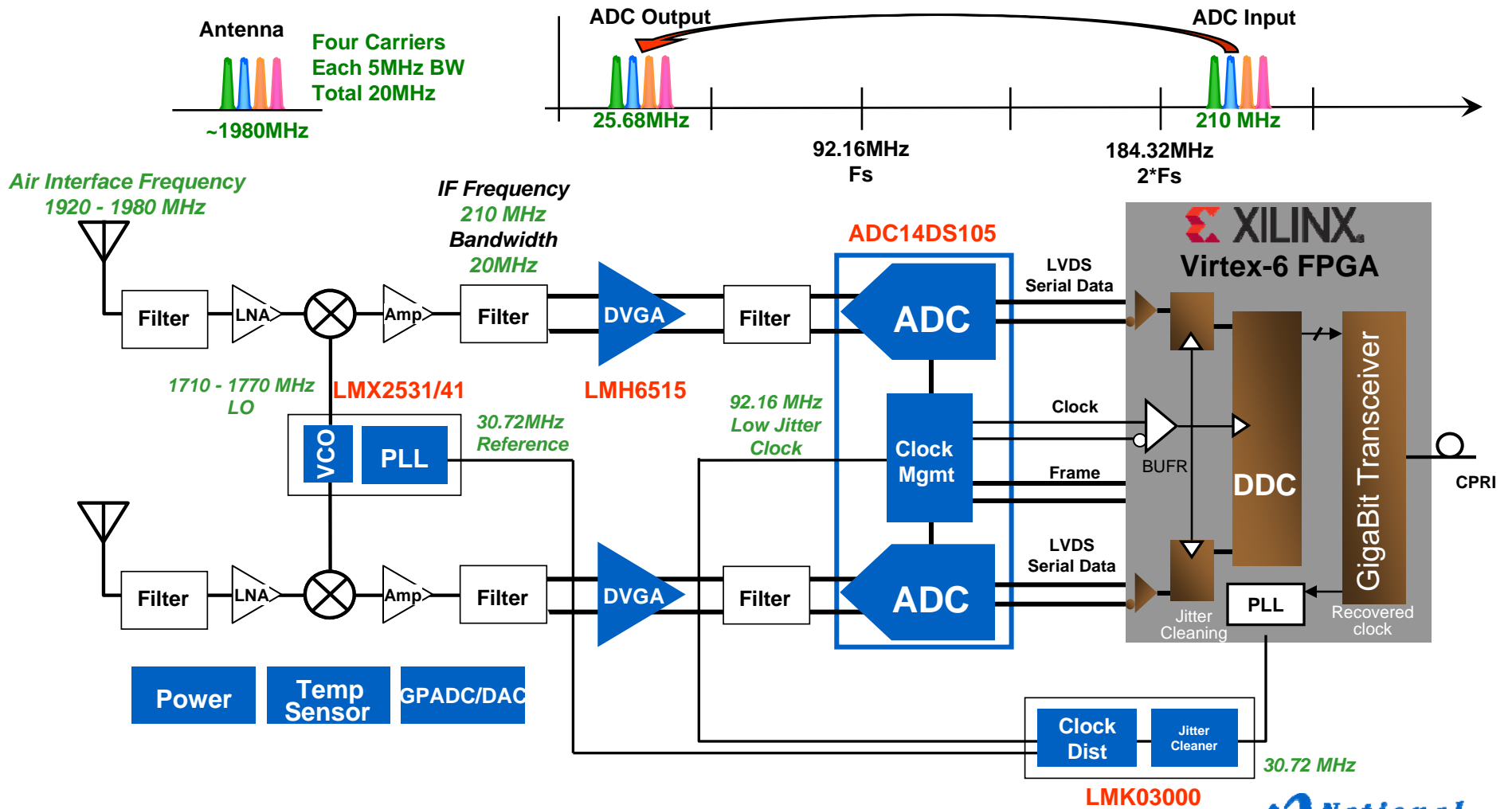


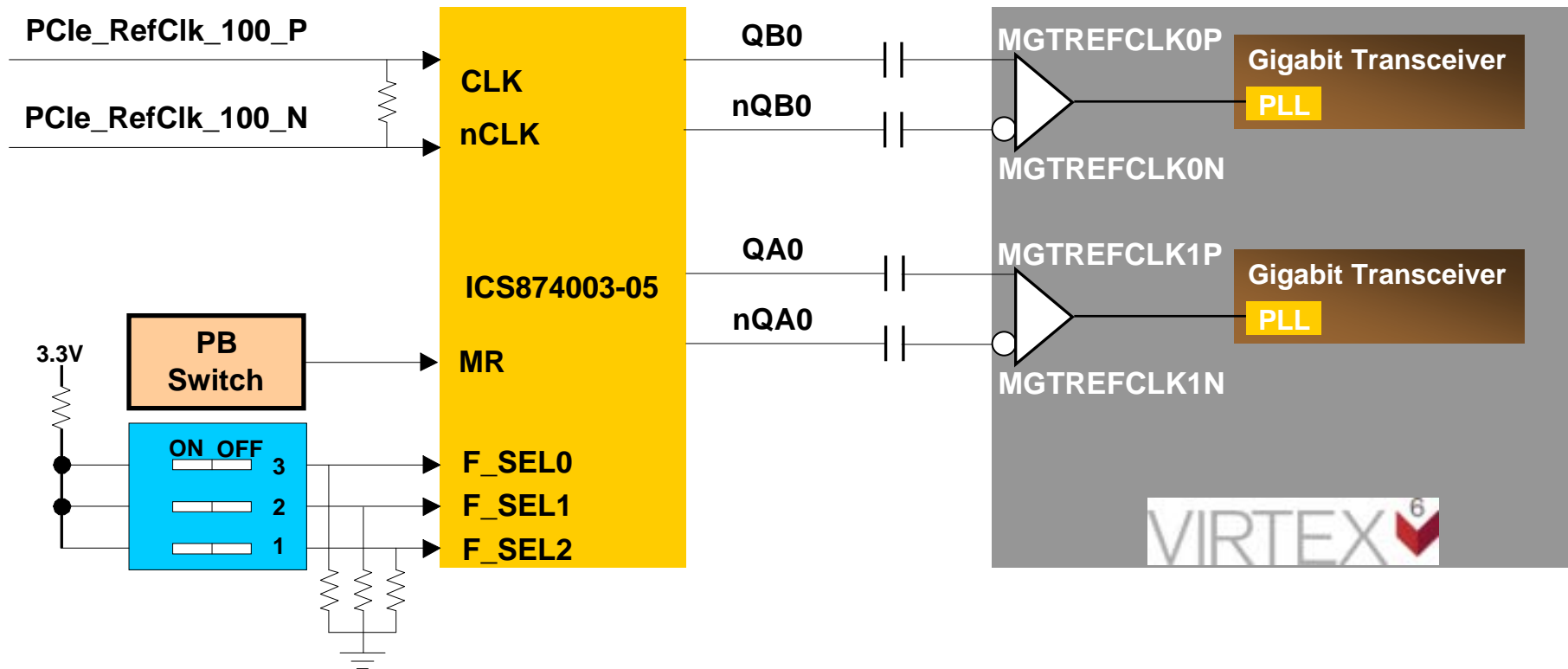
Avnet V5 LX50 Development Board  
[www.em.avnet.com/exp-dac](http://www.em.avnet.com/exp-dac)

ICS8442



Xilinx Virtex-6 ML605 Development Board





**The QA0/nQA0 and QB0/nQB0 outputs can be set to 100MHz, 125MHz, or 250MHz using the F\_SEL[2:0] inputs of the ICS874003-05 device.**

- System-Level Clocking Overview
- High-Performance Clock Generators
- Xilinx FPGA Clocking Resources
- Case Studies
- **Demo**

Choose  
Architecture

Easy Entry of  
Clock  
Frequencies  
and Formats

The screenshot shows the 'National's Clock Design Tool' window. The 'Design Flow' bar at the top indicates the current step is 'Customer Requirements'. The main area is titled 'Customer Requirements' and is divided into three sections:

- Step 1) Select Architecture Type:** Three radio buttons are present: 'Single PLL - LMK03000 and LMK02000 Family', 'Dual PLL', and 'Dual Loop PLL - LMK04000 Family'. The 'Dual Loop PLL' option is selected. Below this is a block diagram showing a Reference input connected to PLL1, which is connected to VCO1 and then to an Output. PLL2 is also connected to VCO2 and then to Output(s).
- Step 2) Inputs:** A 'Reference' input is selected with a radio button. A text box contains '122.88 MHz'. Below this are three radio buttons: 'Manual Entry' (selected), 'Auto select best standard frequency', and 'Auto select best frequency'.
- Step 3) Outputs:** A note states 'Up to eight outputs may be programmed. Blank outputs are ignored.' Eight output configurations are listed:
  - Output #1: 737.28 MHz, Type: LVPECL
  - Output #2: 61.44 MHz, Type: LVCMOS
  - Output #3: 30.72 MHz, Type: LVCMOS
  - Output #4: 30.72 MHz, Type: Don't care
  - Output #5: 61.44 MHz, Type: Don't care
  - Output #6: 61.44 MHz, Type: Don't care
  - Output #7: 61.44 MHz, Type: Don't care
  - Output #8: (blank) MHz, Type: Don't care

At the bottom of the window are 'Next', 'Cancel', and 'Help' buttons. The status bar at the very bottom shows 'Ready' and 'Welcome To National's Clock Design Tool!'.

List of Potential Solutions & Configurations To Select

**National's Clock Design Tool**

File Help

Design Flow: Home Customer Requirements **Select Solution** Select Configuration Simulation

### Select Solution

PLL Part Number	Score	Matches	Layout type	Highest VCXO Freq	Highest PDF2	Lowest VCO Freq	Lowest VCO Divider
LMK04001	100	1	Dual Loop Clock Conditioner	122.88	61.44	1474.56	2

Selected Device Information

Selected layout type image: Dual Loop Clock Conditioner

Block Diagram

Text Info

Next Cancel

Ready Welcome To National's Clock Design Tool!

Easy Device Configuration

The screenshot shows the National's Clock Design Tool interface. At the top, there is a 'Design Flow' bar with icons for Home, Customer Requirements, Select Solution, Select Configuration, and Simulation. Below this, the tool is configured for a 'Custom' design using an 'LMK04001' device and a 'VCXO' oscillator. The main workspace contains several configuration panels:

- CLKin:** Input frequency set to 30.72 MHz.
- PLL1\_R:** Reference divider set to 1.
- PLL1\_N:** PLL1 division factor set to 4.
- PLL1:** Phase-locked loop configuration with PDF (Phase Frequency Divider) set to 30720.0 kHz and CP (Charge Pump) current set to 0.08 mA.
- LOOPFILTER1:** Loop filter configuration with R (kohms) and C (nF) values: R1=330.0, R2=0.0, R3=0.0, R4=0.0; C1=0.022, C2=1.0, C3=0.0, C4=0.0.
- VCXO:** Oscillator configuration with a frequency of 122.88 MHz and a sensitivity of 2.0 kHz/V.
- PLL2\_R:** Reference divider set to 2.
- PLL2\_N:** PLL2 division factor set to 12.
- PLL2:** PLL2 configuration with PDF set to 61440.0 kHz and CP set to 3.2 mA.
- LOOPFILTER2:** Loop filter configuration with R (kohms) and C (nF) values: R1=0.68, R2=0.6, R3=0.2, R4=0.2; C1=0.068, C2=4.7, C3=0.0, C4=0.01.
- VCO:** Voltage-controlled oscillator configuration with a frequency range of 1430.0 to 1570.0 MHz, a center frequency of 1474.56 MHz, and a sensitivity of 8.9549 MHz/V.
- Fout SINEWAVE:** Output filter configuration with a checkbox for SINEWAVE.
- VCODIV:** VCO division factor set to 2.
- DIVIDEO:** Output divider set to 1.
- DELAYO:** Delay mode set to Bypassed.
- CLKout0:** Output driver configuration with a checked box for CLKout0, LVPECL output type, and a frequency of 737.28 MHz.

The status bar at the bottom indicates 'Ready' and 'Welcome To National's Clock Design Tool!'.

PLL Loop Filter Design

The screenshot shows the National's Clock Design Tool interface. A 'Loop Filter Design' dialog box is open, displaying parameters for 'LOOPFILTER1'. The dialog includes sections for 'Loop Filter Parameters', 'Loop Filter Values', and 'Loop Filter Design'.

**Loop Filter Design**

Selected LOOPFILTER: LOOPFILTER1  
 Selected PLL: PLL1  
 Selected VCO: VCXO

**Loop Filter Parameters**

Pick loop filter for me

Design	Achieved
Bandwidth: 1.818 kHz	2.1
Phase Margin: 70.0 degrees	71.711

**Loop Filter Values**

Calculate

R2	330.0 kohms
R3	0.0 kohms
R4	0.0 kohms
C1	0.022 nF
C2	1.0 nF
C3	0.0 nF
C4	0.0 nF

**LOOPFILTER1**

R (kohms)	C (nF)
R1	C1 0.022
R2 330.0	C2 1.0
R3 0.0	C3 0.0
R4 0.0	C4 0.0

**VCXO**

122.88 MHz  
2.0 kHz/V

**LOOPFILTER2**

R (kohms)	C (nF)
R1	C1 0.068
R2 0.68	C2 4.7
R3 0.6	C3 0.0
R4 0.2	C4 0.01

**VCO**

1430.0 to 1570.0  
1474.56 MHz  
8.9549 MHz/V

Fout SINEWAVE

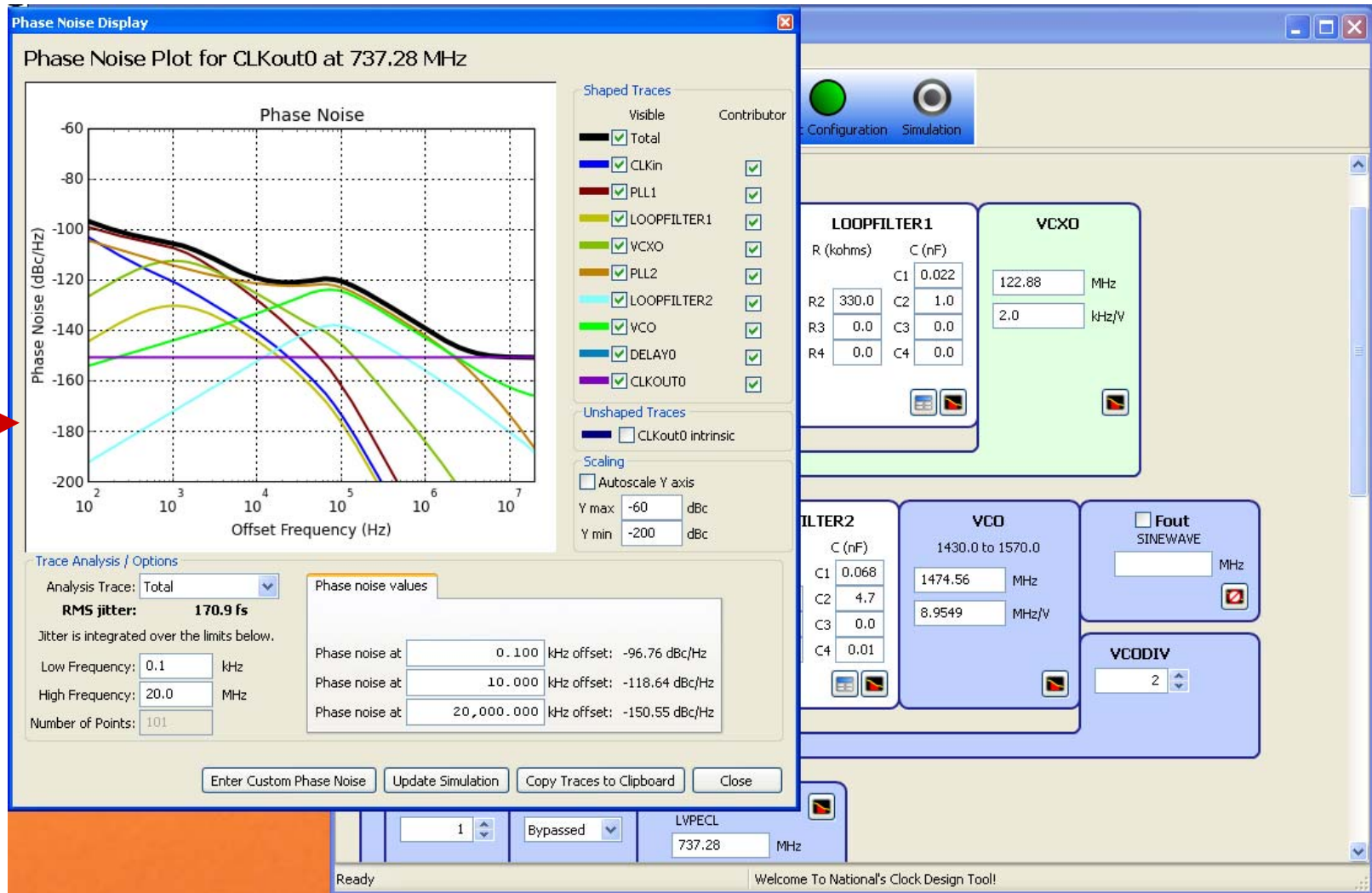
**VCODIV**

2

**Kout0**

1 Bypassed 737.28 MHz

Phase Noise & Jitter Simulations & Analysis



- **Presented system level clocking requirements and performance metrics**
- **Demonstrated industry-leading high-speed clocking solutions**
- **Explored latest Xilinx Virtex-6 and Spartan-6 clocking resources**



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Thanks for coming!



Please Visit the Demo Area!

X-fest General Info:

<http://em.avnet.com/xfest>

X-fest Presentation Questions:

<http://em.avnet.com/xfsupport2010>

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# 2009 Xfest

Supplementary Material

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# LMK01000 Clock Distributor

## 2:8 Clock Buffer, Divider, Distributor (30-fs Additive RMS Jitter)

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### ■ Features & Value Proposition

- Ultra-Low Additive Noise
  - 30-fs of additive RMS noise

### ■ Markets

- Radio Unit of Base Station
- Test & Measurement, Military & Aerospace
- Medical Imaging & Ultra-Sound

NSID	Outputs			Architecture	Output Clock Range (MHz)	VCO Frequency Range (MHz)	RMS Jitter (ps) *
	LVPECL	LVDS	LVC MOS				
LMK01000ISQ	5	3	0	2:10 Clock Distribution	1 – 1600	NA	0.03 (add.)
LMK01010ISQ	0	0	8		1 – 1600	NA	0.03 (add.)
LMK01020ISQ	8	0	0		1 – 1600	NA	0.03 (add.)

\* Jitter integrated from 12 kHz to 20 MHz





# LMK03000 Clock Generator

Clock Generator with Internal VCO (<200-fs Additive RMS Jitter)

*Accelerating Your Success™*



- **Value Proposition**
  - <200-fs Additive RMS Jitter for Clock Generation
- **Applications**
  - Test & Measurement, Military & Aerospace
  - Medical Imaging & Ultra-Sound

NSID	Outputs			Architecture	Output Clock Range (MHz)	VCO Frequency Range (MHz)	RMS Jitter (ps) *
	LVPECL	LVDS	LVC MOS				
LMK03000DISQ	5	3	0	PLL + VCO + Clock Distribution	1 – 648	1185 – 1296	0.8/0.4/1.2
LMK03001DISQ	5	3	0		1 – 785	1470 – 1570	0.8/0.4/1.2
LMK03002DISQ	4	0	0		1 – 860	1566 – 1724	0.8/0.4/1.2
LMK03033DISQ	4	4	0		1 – 1080	1840 – 2160	0.8/0.5/1.2

\* Jitter integrated from 12 kHz to 20 MHz





# LMK03000 Clock Jitter Cleaner

## Clock Jitter Cleaner with Internal VCO (400 to 1200-fs RMS Jitter)

*Accelerating Your Success™*



- **Value Proposition**
  - Low-Noise VCO
- **Applications**
  - Baseband Unit of Wireless Infrastructure
  - 10/40/100Gbps Optical Transceivers

NSID	Outputs			Architecture	Output Clock Range (MHz)	VCO Frequency Range (MHz)	RMS Jitter (ps) *
	LVPECL	LVDS	LVC MOS				
LMK03000/C/DISQ	5	3	0	PLL + VCO + Clock Distribution	1 – 648	1185 – 1296	0.8/0.4/1.2
LMK03001/C/DISQ	5	3	0		1 – 785	1470 – 1570	0.8/0.4/1.2
LMK03002/C/DISQ	4	0	0		1 – 860	1566 – 1724	0.8/0.4/1.2
LMK03033/C/DISQ	4	4	0		1 – 1080	1840 – 2160	0.8/0.5/1.2

\* Jitter integrated from 12 kHz to 20 MHz





# LMK02000 Clock Jitter Cleaner

## Clock Jitter Cleaner with External VCXO (20-fs Additive RMS Jitter)

70

*Accelerating Your Success™*



### ■ Features & Value Proposition

- Low-Noise PLL and Distribution
  - 20-fs of additive RMS noise

### ■ Applications

- Radio Unit of Base Station
- Test & Measurement, Military & Aerospace
- Medical Imaging & Ultra-Sound

NSID	Outputs			Architecture	Output Clock Range (MHz)	VCO Frequency Range (MHz)	RMS Jitter (ps) *
	LVPECL	LVDS	LVC MOS				
LMK02000ISQ	5	3	0	PLL + Clock Distribution (VCXO)	1 – 860	NA	0.2 (+VCXO)
LMK02002ISQ	4	0	0		1 – 860	NA	0.2 (+VCXO)

\* Jitter integrated from 12 kHz to 20 MHz



# LMK04000 Clock Jitter Cleaner

Clock Jitter Cleaner with External VCXO/Crystal (<200-fs RMS Jitter)

Accelerating Your Success™



- **Features & Value Proposition**
  - <200-fs RMS Jitter for Clock Generation
- **Applications**
  - Test & Measurement, Military & Aerospace
  - Medical Imaging & Ultra-Sound

NSID	Outputs			Architecture	Output Clock Range (MHz)	VCO Frequency Range (MHz)	RMS Jitter (ps) *
	LVPECL	LVDS	LVC MOS				
LMK04000BISQ	3	0	4	Cascaded PLLs + VCO + Clock Distribution (needs external crystal or VCXO in PLL1)	1 – 648	1185 – 1296	0.2 (+XO)
LMK04001BISQ	3	0	4		1 – 785	1430 – 1570	0.2 (+XO)
LMK04011BISQ	5	0	0		1 – 785	1430 – 1570	0.2 (+XO)
LMK04031BISQ	2	2	2		1 – 785	1430 – 1570	0.2 (+XO)
LMK04002BISQ	3	0	4		1 – 875	1566 – 1750	0.2 (+XO)
LMK04033BISQ	2	2	2		1 – 1080	1840 – 2160	0.2 (+XO)

\* Jitter integrated from 100 Hz to 20 MHz

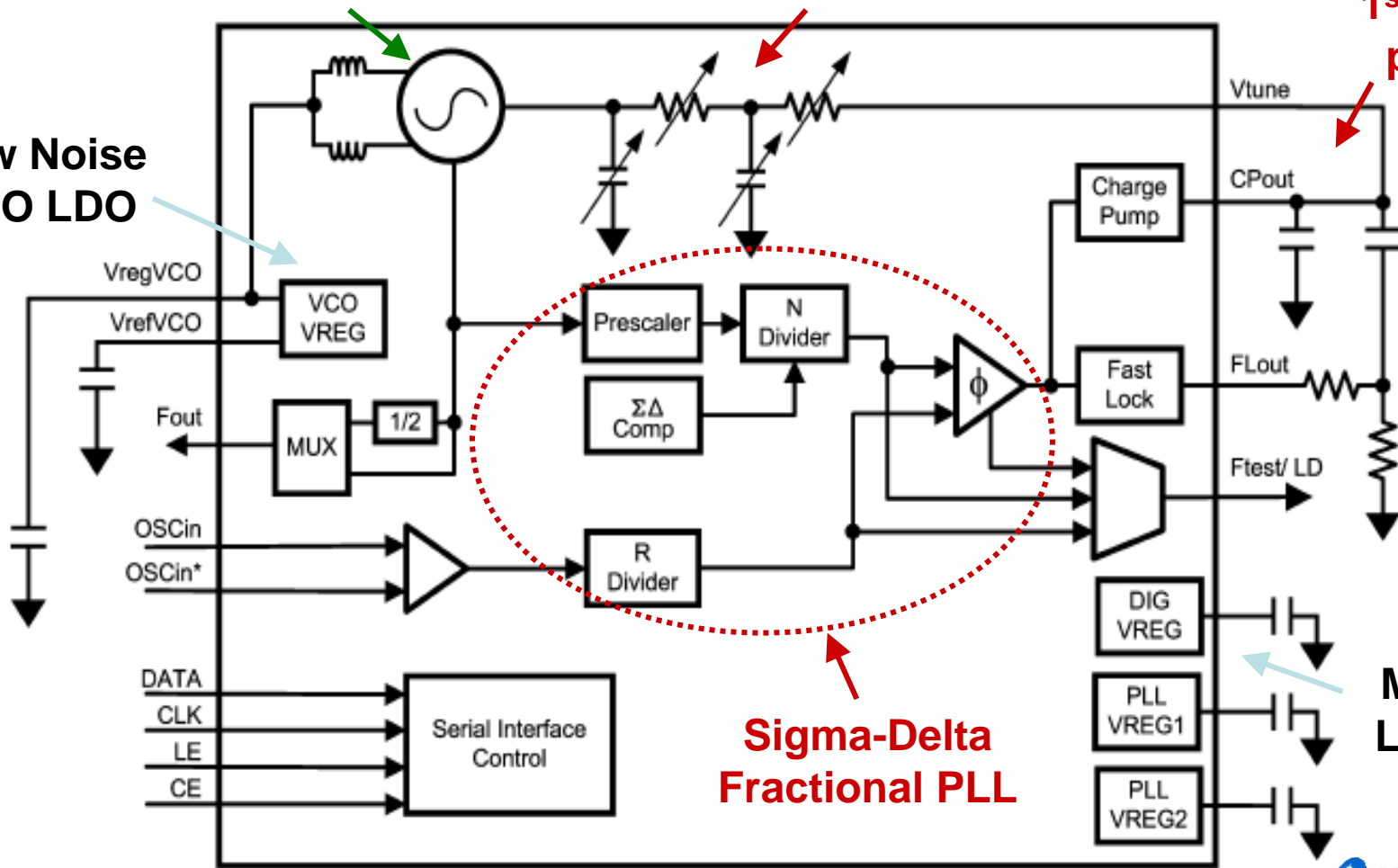


Integrated Low-Noise VCO

Programmable 3<sup>rd</sup> and 4<sup>th</sup> poles

1<sup>st</sup> & 2<sup>nd</sup> poles

Low Noise VCO LDO



Sigma-Delta Fractional PLL

More LDOs

## Existing Devices

Part No.	Low Band (MHz)	High Band (MHz)
LMX2531LQ1500E	749.5 – 755	1499 – 1510
LMX2531LQ1570E	765 – 818	1530 – 1636
LMX2531LQ1650E	795 – 850	1590 – 1700
LMX2531LQ1700E	831 – 865	1662 – 1770
LMX2531LQ1778E	863 – 920	1726 – 1840
LMX2531LQ1742	880 – 933	1760 – 1866
LMX2531LQ1910E	917 – 1014	1834 – 2028
LMX2531LQ2080E	952 – 1137	1904 – 2274
LMX2531LQ2265E	1089 – 1200	2178 – 2400
LMX2531LQ2570E	1168 – 1395	2336 – 2790

## Recent releases & devices under development

Part No.	Low Band (MHz)	High Band (MHz)	Sample Date	Release Date
LMX2531LQ1146E	553 – 592	1106 – 1184	NOW	NOW
LMX2531LQ1226E	592 – 634	1184 – 1268	NOW	NOW
LMX2531LQ1314E	634 – 680	1268 – 1360	NOW	NOW
LMX2531LQ1415E	680 – 735	1360 – 1470	NOW	NOW
LMX2531LQ1515E	725 – 790	1450 – 1580	NOW	NOW
LMX2531LQ2820E	1355 – 1462	2710 – 2925	Oct	Feb 09
LMX2531LQ3010E	1455 – 1566	2910 – 3132	Dec	Feb 09

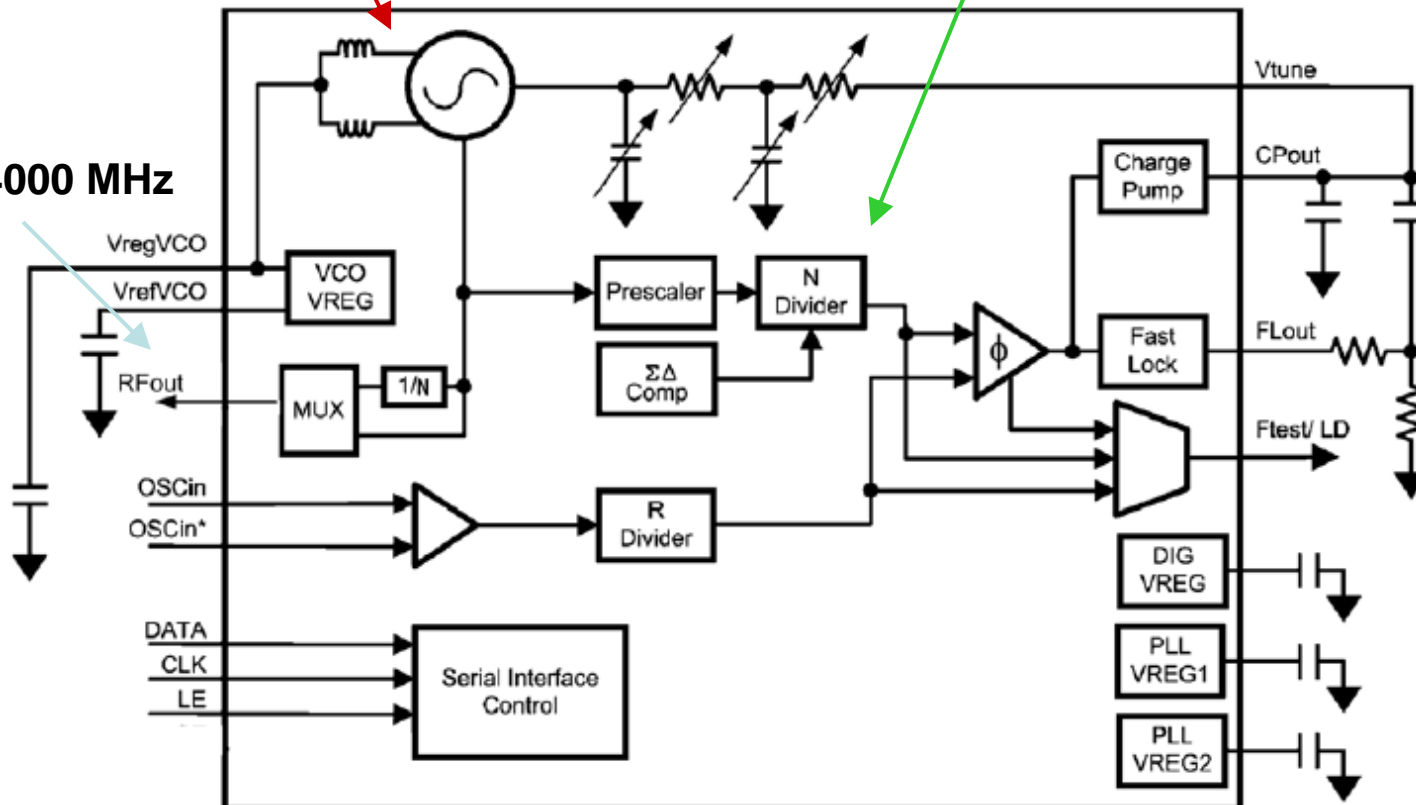


- **Ultra Low-Noise PLL**
  - Integer Mode (-224 dBc/Hz)
  - Fractional Mode (-223 dBc/Hz)
    - Programmable 4<sup>th</sup> order  $\Delta\Sigma$  Modulator
  - 100 MHz Phase Detector Rate
  - Can be Used as Stand-Alone PLL (VCO bypass mode)
  
- **Very Wide Frequency Range**
  - 30 MHz to 4000 MHz continuous coverage
    - 6 parts & odd/even divides up to 63 with 50% duty cycle
    - See table for detail coverage per device

VCO: 1.9 – 4 GHz  
(with 6 devices)

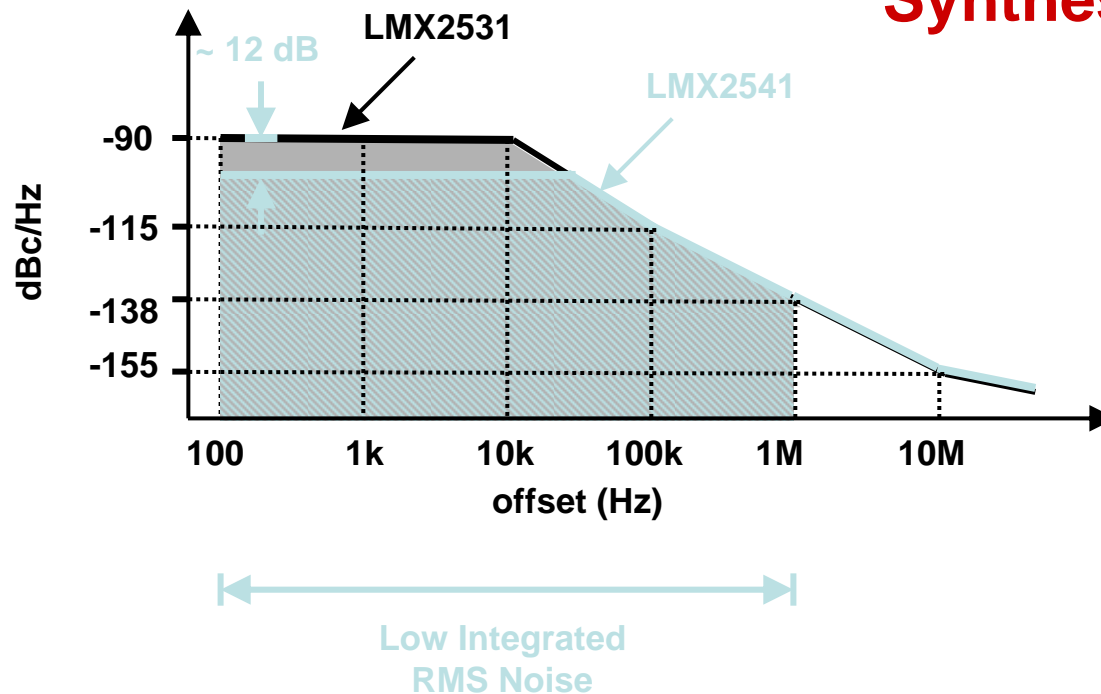
Ultra Low-Noise PLL

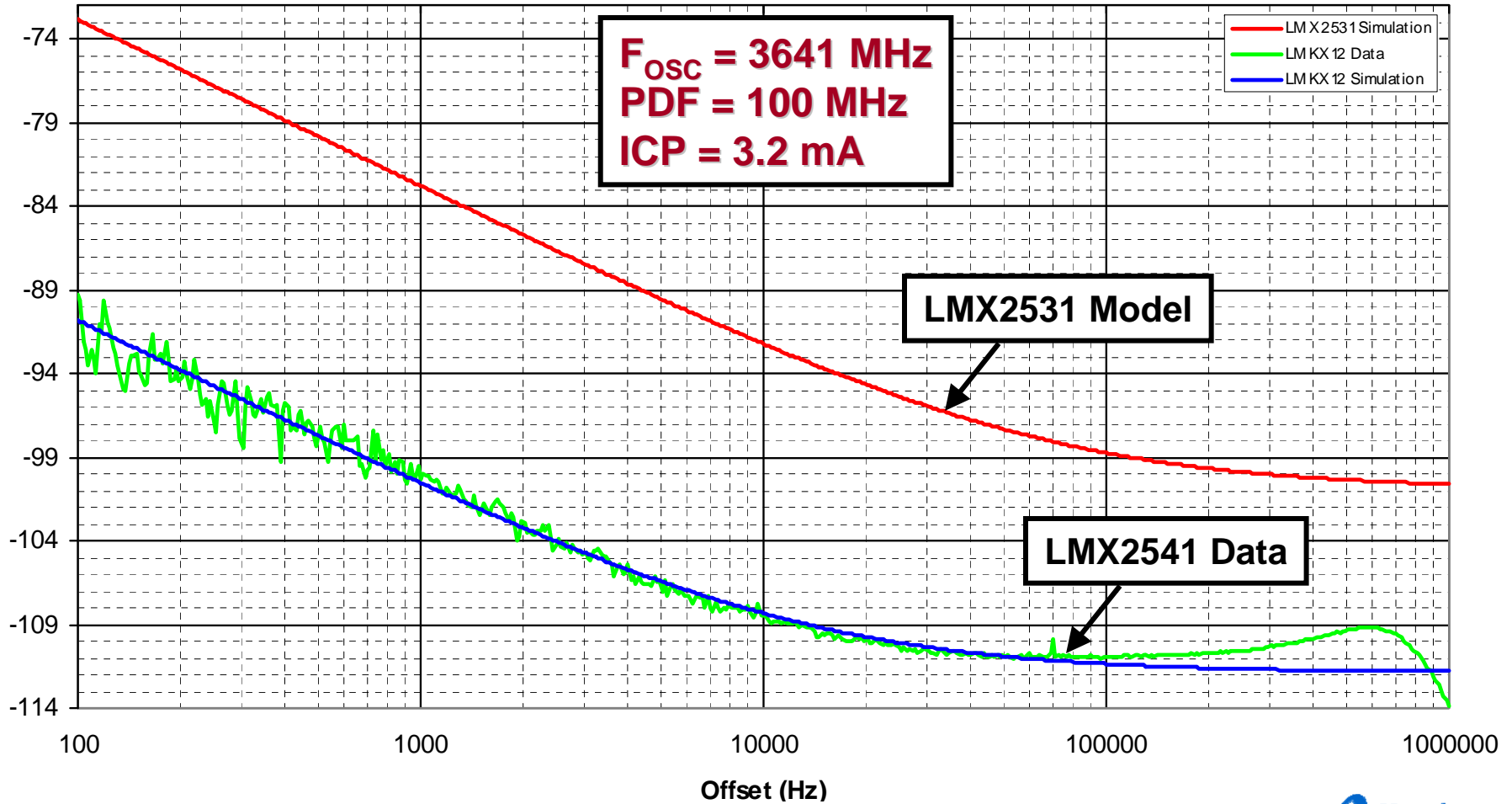
50 – 4000 MHz



- Phase Noise at  $F_{osc} = 2\text{ GHz}$

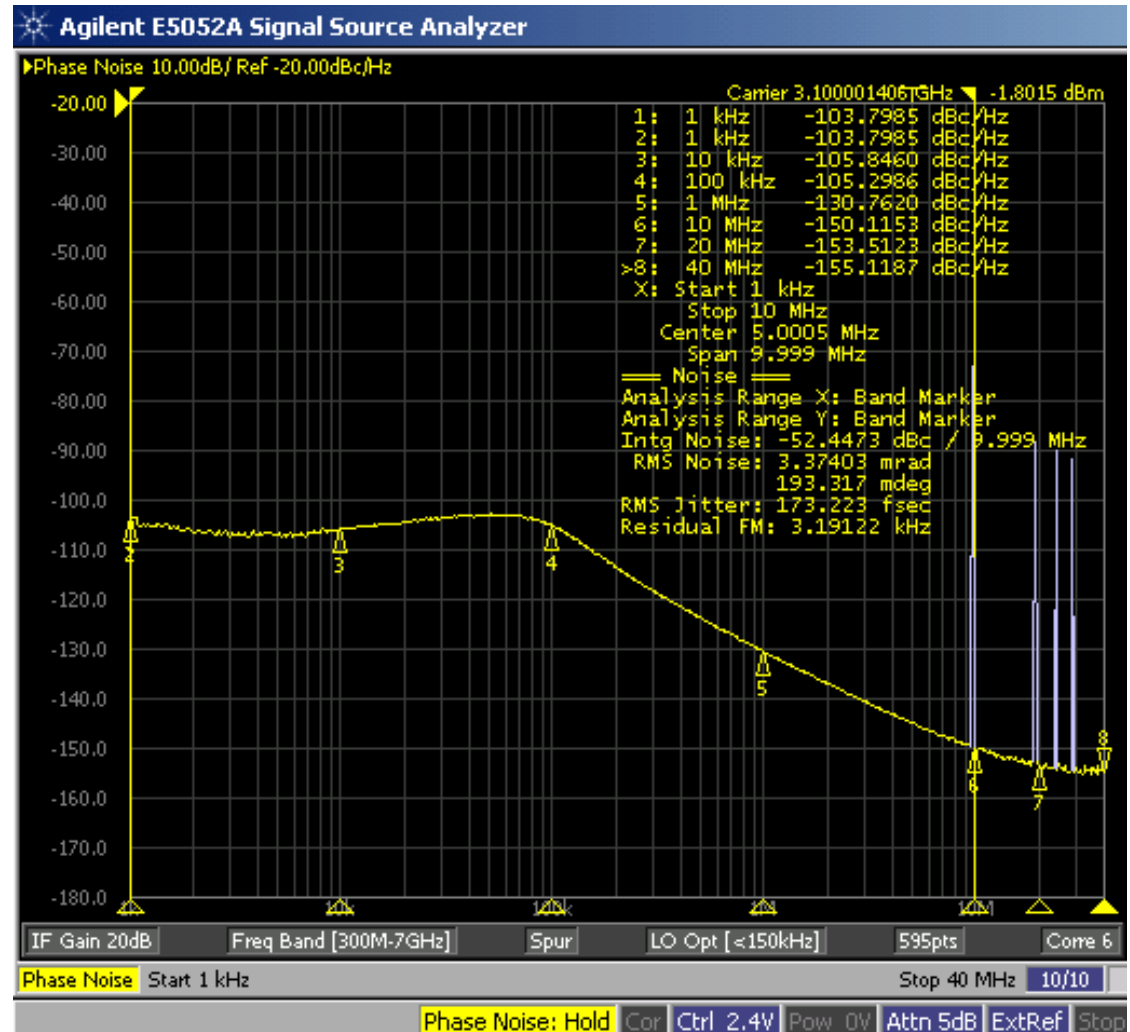
**Industry's  
Lowest Noise  
Synthesizer**





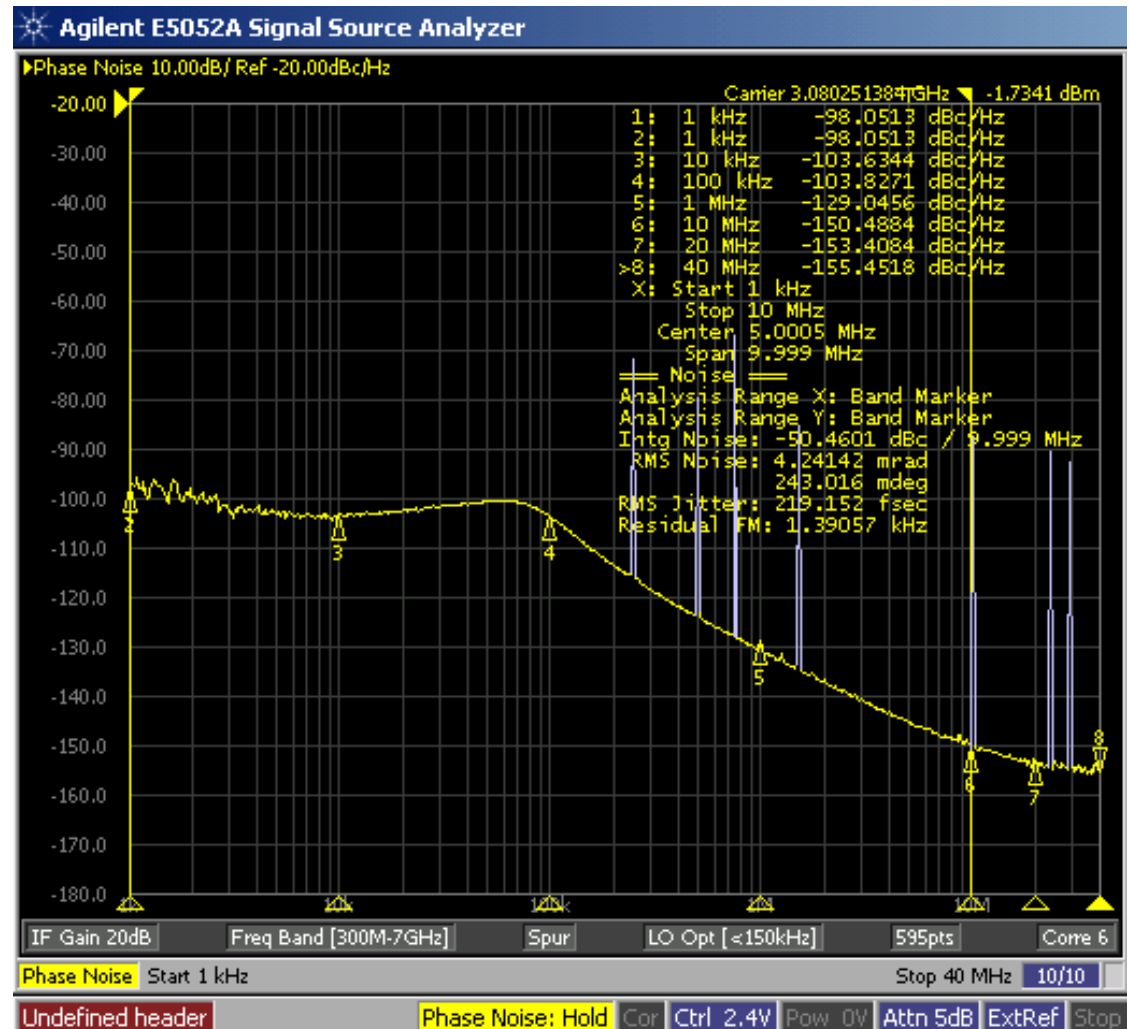
→ Integer Mode  
 FVCO = 3100 MHz  
 FPD = 100 MHz  
 ICP = 3.2 mA

**PLL Noise = -224 dBc/Hz**  
**RMS Noise = 3.4 mrad**  
 (1 kHz – 20 MHz)



→ Fractional Mode  
 FVCO = 3080 MHz  
 FPD = 100 MHz  
 ICP = 2.5 mA  
 Channel Spacing = 250 kHz

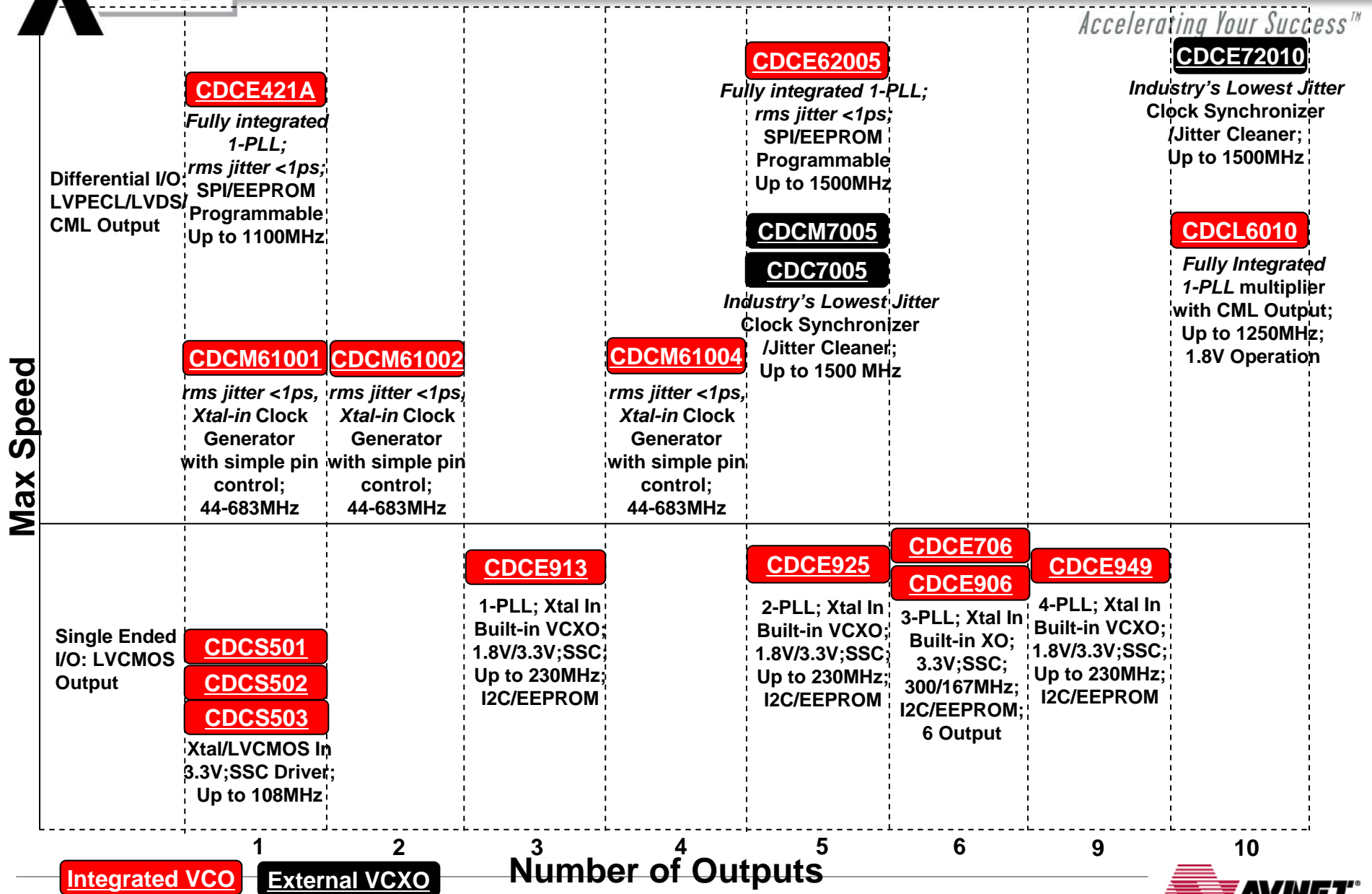
**Spurs = -65 dBc**  
**RMS Noise = 4.2 mrad**  
 (1 kHz – 20 MHz)



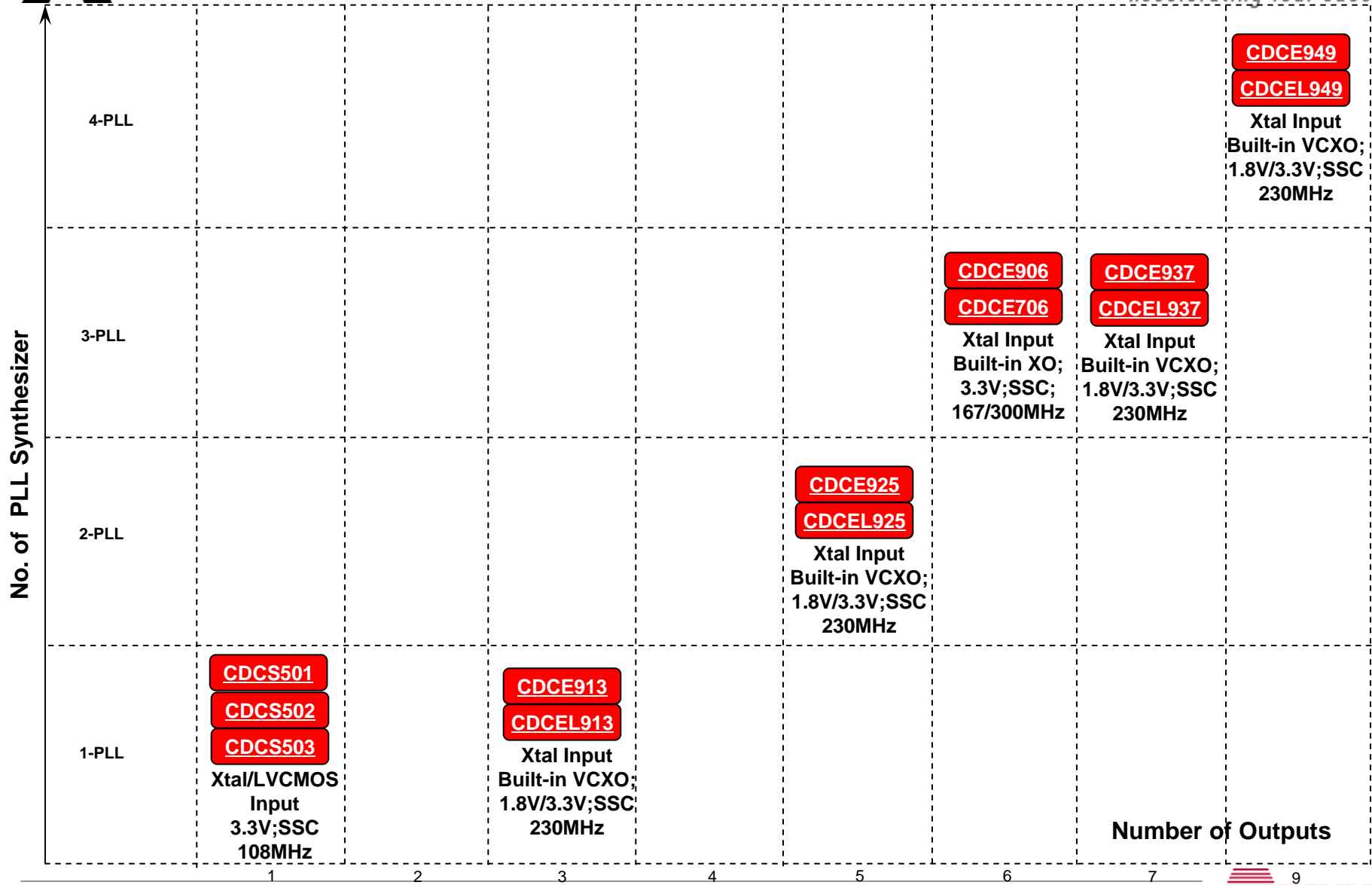




# TI General Purpose Synthesizer Featured Products



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Number of Outputs

## Features

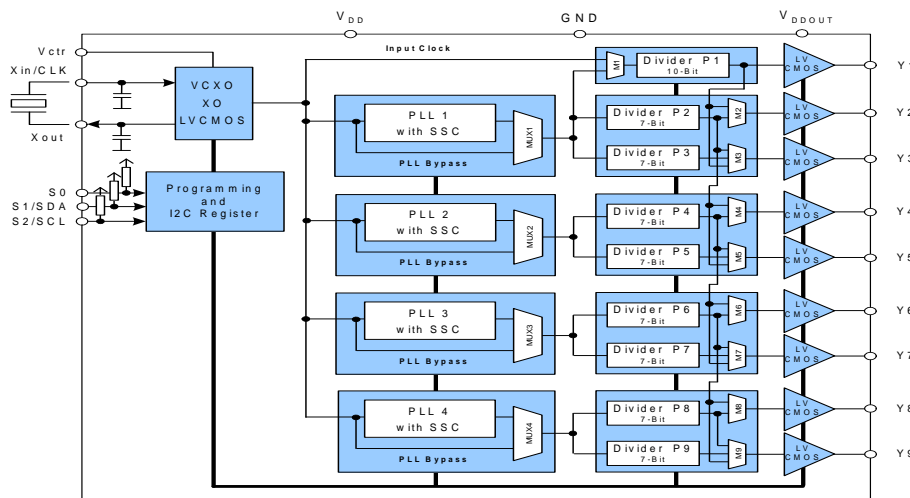
- Input Clock: LVCMOS (160 MHz) and Crystal (8- 32MHz)
- VCXO input with  $\pm 150$ ppm (typ) pulling range
- Output frequencies up to 230 MHz @ 1.8V, 2.5V and 3.3V
- 9 low-jitter, low-skew high-performance outputs
- Three user-definable control inputs
- Spread-Spectrum Clocking
- On-chip EEPROM
- 1.8V supply voltage, 3.3V or 2.5V I/O for CDCE949 and 1.8V I/O for CDCEL949

## Benefits

- Wide I/O frequency range supports wide frequency ratio for Audio/Video clocking
- Enables Zero PPM clocking generation
- Supports frequency scaling and power saving
- Reduce EMI noise
- Easy to customize by EEPROM-Lock
- 1.8V ready – low power consumption
- 24 Pin TSSOP

## Applications

- Digital Media Systems (Audio/Video)
- DSP, DaVinci and OMAP Attached
- IP-STB/TV/Phone
- Streaming Media (i.e. DVD-P/R)
- Automotive Entertainment
- Portable Media
- Print Media



CDCE949PERF-EVM / CDCEL949PERF-EVM  
CDCEL9xxPROG-EVM

1Ku / \$2.20

### Features

- Wide Input/Output freq. range
  - 40 - 115 MHz for 501
  - 8 – 32MHz Input/8-108MHz Output for 503
- Selectable Spread-Spectrum Modulation of  $\pm 0.0\%$ ,  $\pm 0.5\%$ ,  $\pm 1.0\%$ , and  $\pm 2.0\%$
- Selectable frequency multiplication rates of 1x and 4x (CDCS503 only)
- 8 pin TSSOP package
- Operation condition: Single 3.3V power supply, wide temperature range -40 , 85

### Benefits

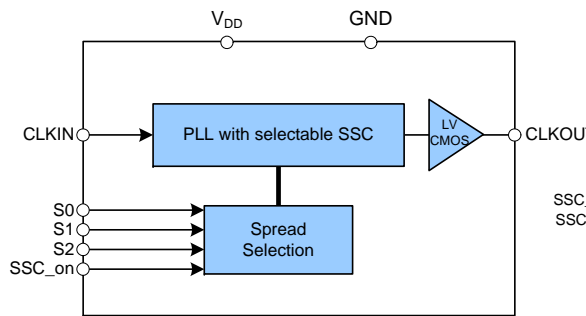
- • Saves BOM: single device covers multiple designs
- • Reduce EMI thru selectable amount of SSC modulation up to 10dB
- • Saves component for higher frequency XO
- • Small board space
- • Simple power supply scheme; applicable to wider applications with better reliability

### Applications

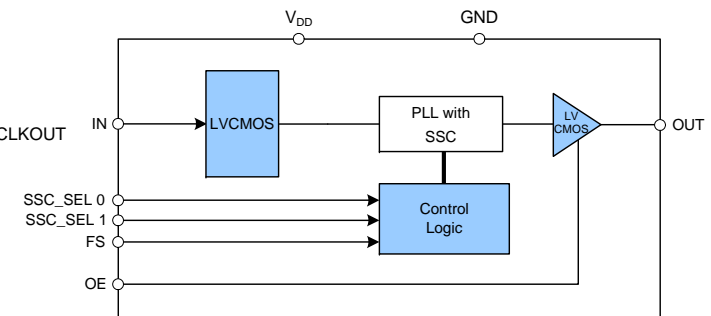
General purpose clock driver with EMI reduction capability:

- Audio/Video entertainment
  - Flat Panel TV; Set-top Boxes;
  - Blu-Ray DVDR
- Printers; PCs
- Communications access point/gateway/networking card
- Industrial

1Ku: \$0.45/\$0.50



CLKIN	1	8	V <sub>DD</sub>
S0	2	7	S2
S1	3	6	CLKOUT
GND	4	5	SSC_on



X <sub>IN</sub>	1	8	V <sub>DD</sub>
SSC_SEL 0	2	7	OE
SSC_SEL 1	3	6	OUT
GND	4	5	FS



## Features

- 1:10 Differential LVPECL Clock Outputs with Frequency Range From DC to 3.5 GHz
- Supply Voltage Range From 2.375 V to 3.8 V
- Low-Output Skew (Typ 15 ps)
- Input Mux
- LVDS, CML, SSTL input compatible
- VBB Reference Voltage Output for Single-Ended Clocking
- Available in the QFN32 and LQFP32 Package
- Pin-to-Pin Compatible With MC100 Series LVEP111, EP111, ES6111, PTN1111

## Applications

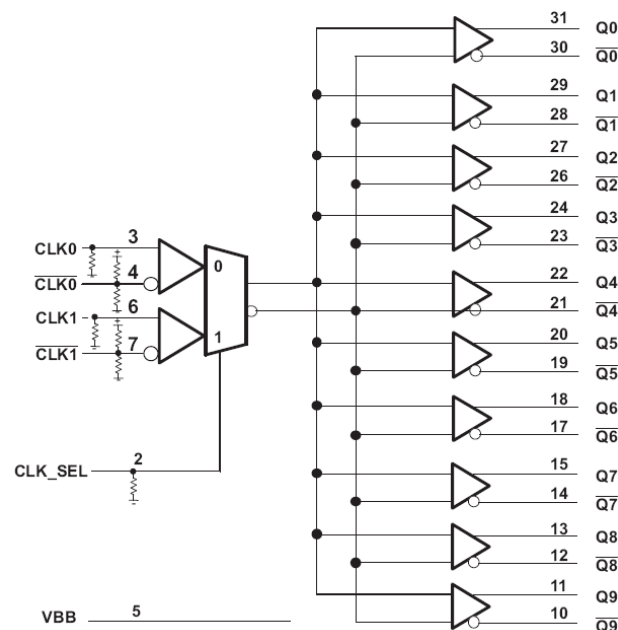
High quality clock distribution for:

- Wireless BTS  
(Pico cell, WiMax, Macro Base band)
- Data Communications
- Medical
- Test Equipment

1Ku: \$6.15

## Benefits

- Wide range supports various applications and use one single device across multiple designs.
- Wide supply voltage saves additional cost on LDO
- Low skew ensures high quality clock distribution
- Input allows flexibility
- Enables good quality single ended distribution for design flexibility
- Small package saves board real estate
- Drop-in replacement for competition



### Features

- 2x 5 Differential LVPECL Clock Outputs with Frequency Range From DC to 3.5 GHz
- Supply Voltage Range From 2.375 V to 3.8 V
- Low-Output Skew (Typ 15 ps)
- VBB Reference Voltage Output for Single-Ended Clocking
- Available in the QFN32 Package
- Pin-to-Pin Compatible With the On-semi MC100 Series EP210, LVEP210 (Drop in)

### Benefits

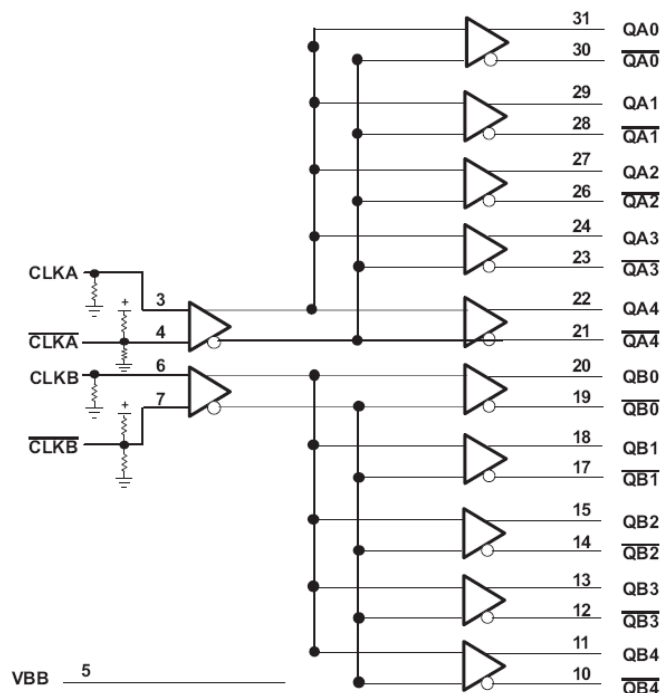
- **Wide range supports various applications and use one single device across multiple designs.**
- **Wide supply voltage saves additional cost on LDO**
- **Low skew ensures high quality clock distribution**
- **Enables good quality single ended distribution for design flexibility**
- **Small package saves board real estate**
- **Drop-in replacement for competition**

### Applications

High quality clock distribution for:

- **Wireless BTS**  
(Pico cell, WiMax, Macro Base band)
- **Data Communications**
- **Medical**
- **Test Equipment**

1Ku: \$6.15





# TI New PECL Translation Logic

*Accelerating Your Success™*

ON Semi Device		Mircel Device		TI Device	
98 (100) Units / Rail	2500 / Tape & Reel	98 Units / Rail	2500 / Tape & Reel	80 Units / Tube	2500 / Tape & Reel
MC10(0)LVEP11D(G)	MC10(0)LVEP11DR2(G)	SY10(0)EL11VZG	SY10(0)EL11VZGTR	SN65LVEP11D	SN65LVEP11DR
MC10(0)LVEP11DT(G)	MC10(0)LVEP11DTR2(G)	-	-	SN65LVEP11DGK	SN65LVEP11DGKR
MC10(0)EL11D(G)	MC10(0)EL11DR2(G)	-	-	SN65EL11D	SN65EL11DR
MC10(0)EL11DT(G)	MC10(0)EL11DTR2(G)	-	-	SN65EL11DGK	SN65EL11DGKR
MC100LVEL11D(G)	MC100LVEL11DR2(G)	-	-	SN65LVEL11D	SN65LVEL11DR
MC100LVEL11DT(G)	MC100LVEL11DTR2(G)	-	-	SN65LVEL11DGK	SN65LVEL11DGKR
MC10(0)EL16D(G)	MC10(0)EL16DR2(G)	SY10(0)EL16VZG	SY10(0)EL16VZGTR	SN65EL16D	SN65EL16DR
MC10(0)EL16DT(G)	MC10(0)EL16DTR2(G)	SY10(0)EL16VKG	SY10(0)EL16VKGTR	SN65EL16DGK	SN65EL16DGKR
MC10(0)ELT22D(G)	MC10(0)ELT22DR2(G)	SY10(0)ELT22LZG	SY10(0)ELT22LZGTR	SN65ELT22D	SN65ELT22DR
MC10(0)ELT22DT(G)	MC10(0)ELT22DTR2(G)	-	-	SN65ELT22DGK	SN65ELT22DGKR
MC100EPT22D(G)	MC100EPT22DR2(G)	SY100EPT22VZG	SY100EPT22VZGTR	SN65EPT22D	SN65EPT22DR
MC100EPT22DT(G)	MC100EPT22DTR2(G)	SY100EPT22VKG	SY100EPT22VKGR	SN65EPT22DGK	SN65EPT22DGKR
MC100LVELT22D(G)	MC100LVELT22DR2(G)	-	-	SN65LVELT22D	SN65LVELT22DR
MC100LVELT22DT(G)	MC100LVELT22DTR2(G)	-	-	SN65LVELT22DGK	SN65LVELT22DGKR
MC10(0)ELT20D(G)	MC10(0)ELT20DR2(G)	SY100ELT20VGZ	SY100ELT20VGZTR	SN65ELT20D	SN65ELT20DR
MC10(0)ELT20DT(G)	MC10(0)ELT20DTR2(G)	-	-	SN65ELT20DGK	SN65ELT20DGKR



### Features

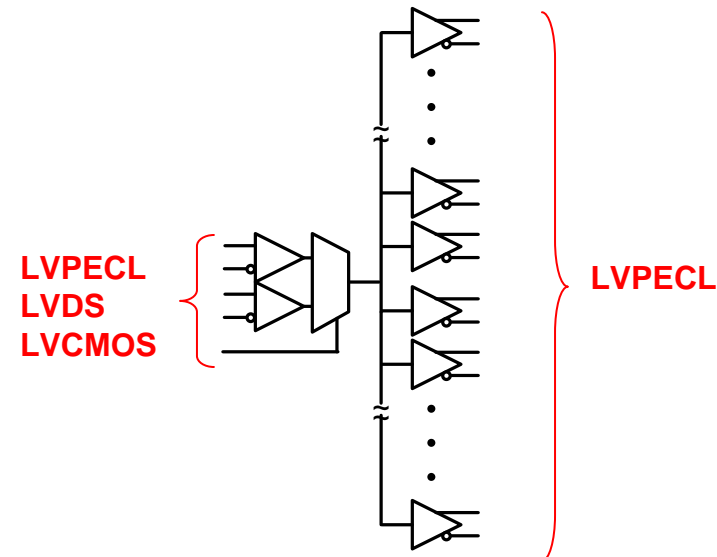
- Total Additive Jitter <100 fs, RMS
- Low-Output Skew 15/20/25/30 ps, maximum
- Signaling Rate Up to 3GHz (min)
- Differential Input Stage for Wide Common-Mode Range
- QFN-16/28/40/48 Package
- Operating conditions of 2.375 to 3.6 V, -40 to 85 C
- Low core current of 60/80/100/120 mA
- Universal Inputs (LVDS, LVPECL, LVCMOS/TTL)
- VBB pin for single ended operation

### Applications

- Applications
  - Router/Switch
  - Datacom/Telecom
  - Wireless Infrastructure
  - Medical
  - Networking
  - General Purpose Differential clock buffering

### Benefits

- Minimal impact on clock quality during distribution
- Better timing control among all outputs
- Single device across multiple designs
- Saves additional interface logic/external components
- Pin-pin compatible allows the same hardware strapping
- More application with improved reliability
- Power efficient
- Saves additional level translation logic
- Improved signal integrity when differential is not used



## Dual Channel 1:2/4/6/8 Universal-to-LVPECL Fan Out Buffer

*Accelerating Your Success™*

### Features

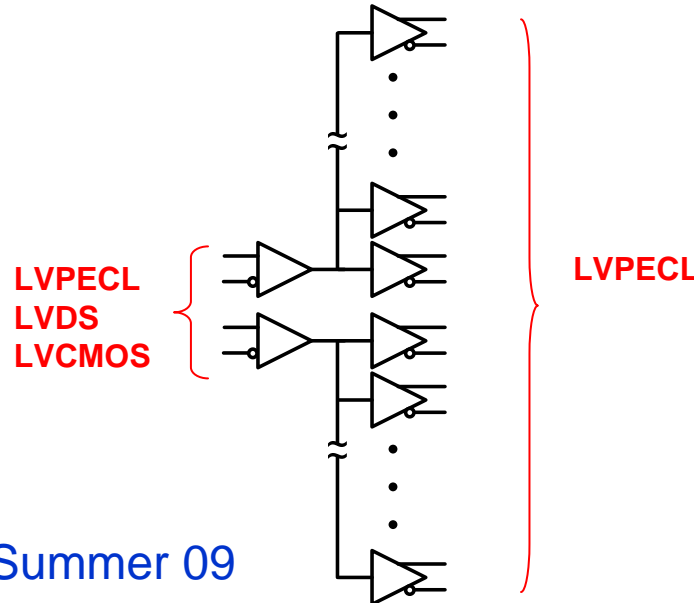
- Total Additive Jitter <100 fs, RMS
- Low-Output Skew 15/20/25/30 ps, maximum
- Signaling Rate Up to 3GHz (min)
- Differential Input Stage for Wide Common-Mode Range
- QFN-16/28/40/48 Package
- Operating conditions of 2.375 to 3.6 V, -40 to 85 C
- Low core current of 60/80/100/120 mA
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- VBB pin for single ended operation

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- Improved signal integrity when differential is not used

### Applications

- Applications
  - Router/Switch
  - Datacom/Telecom
  - Wireless Infrastructure
  - Medical
  - Networking
  - General Purpose Differential clock buffering



Release: Summer 09

### Features

- Operating Frequency: 24 MHz to 200 MHz
- Low Jitter (Cycle-cycle): <|150 ps| Over the Range 66 MHz–200 MHz
- Distributes One Clock Input to One Bank of Five Outputs
- Three-States Outputs When There Is no Input Clock
- Operates From Single 3.3-V Supply
- Available in 8-Pin TSSOP and 8-Pin SOIC Packages
- Internal Feedback Loop Is Used to Synchronize the Outputs to the Input Clock

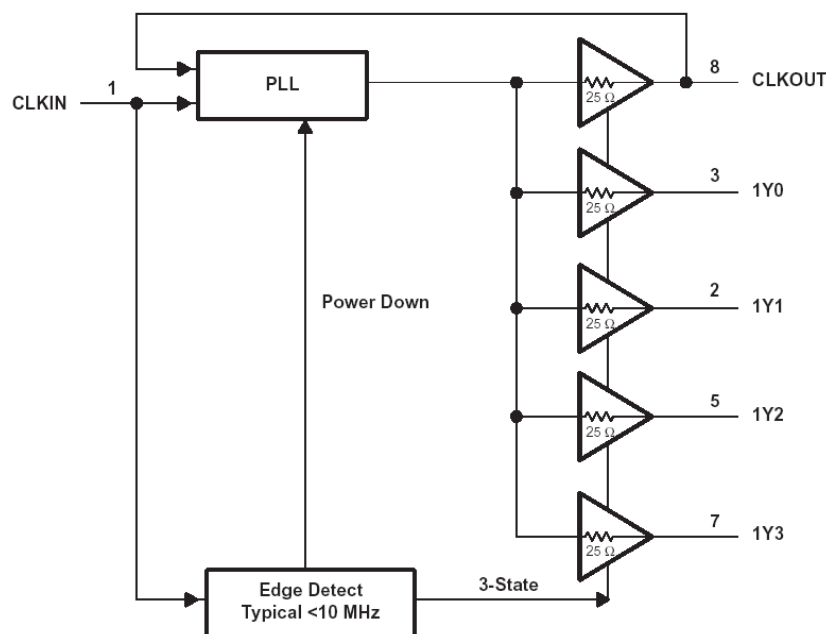
### Applications

- General purpose clock buffer
- Synchronous DRAM
- Duty Cycle Correction

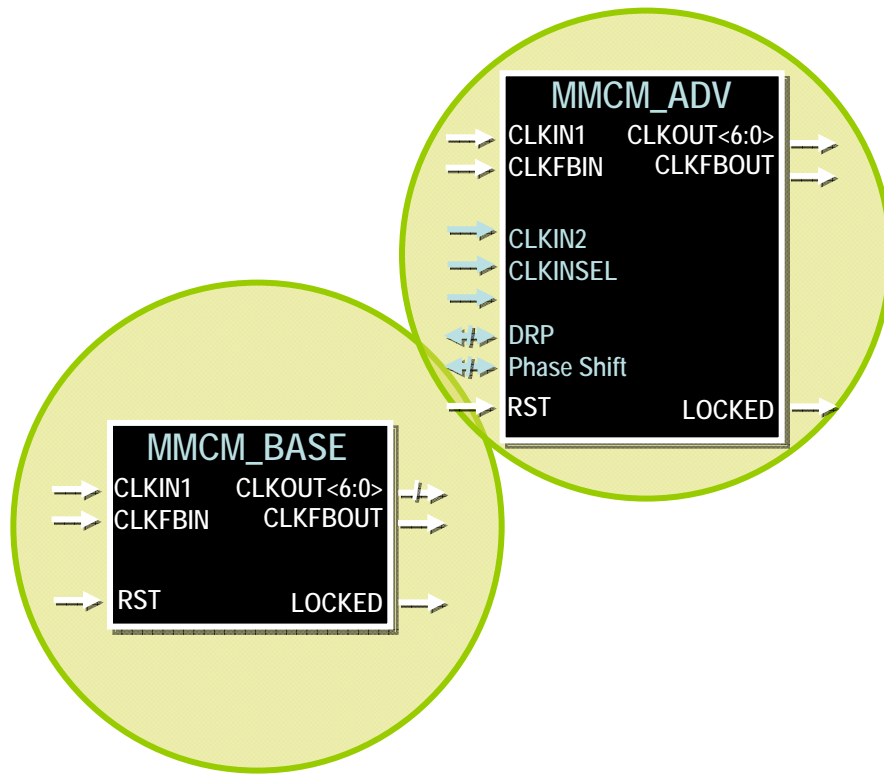
1Ku / \$0.75

### Benefits

- Integrated RC PLL Loop Filter Eliminates the Need for External Components
- Spread Spectrum Clock Compatible
- 25- On-Chip Series Damping Resistors to reduce EMI.





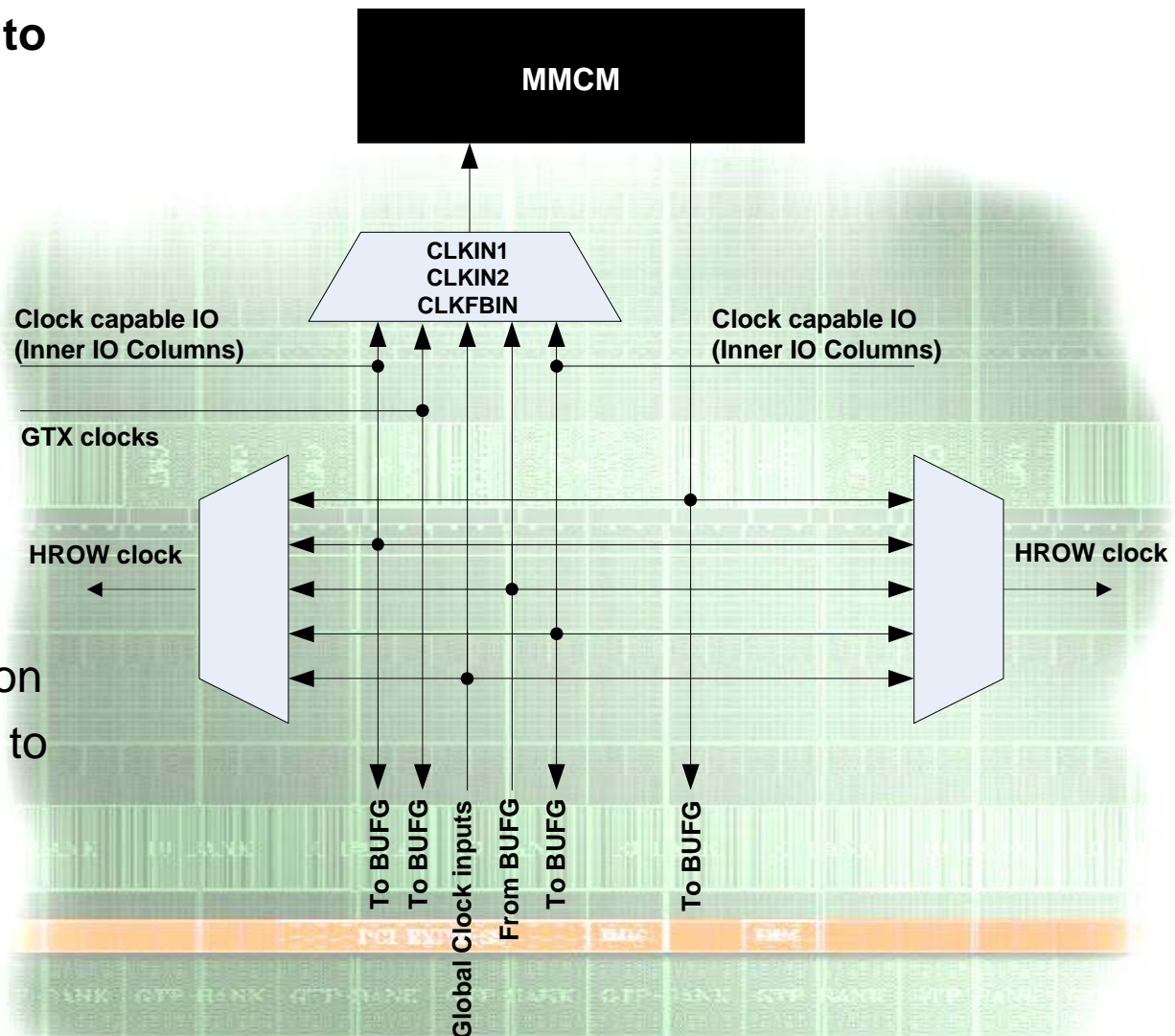


- **Two software primitives**
  - MMCM\_BASE has only the basic ports
  - MMCM\_ADV provides access to all ports
  
- **Eight independently programmable clock outputs**
  - O0 to O6 plus CLKFBOUT
  
- **Additional MMCM\_ADV features**
  - Clock Input Switching
  - Phase Shift Port
  - Dynamic Reconfiguration Port

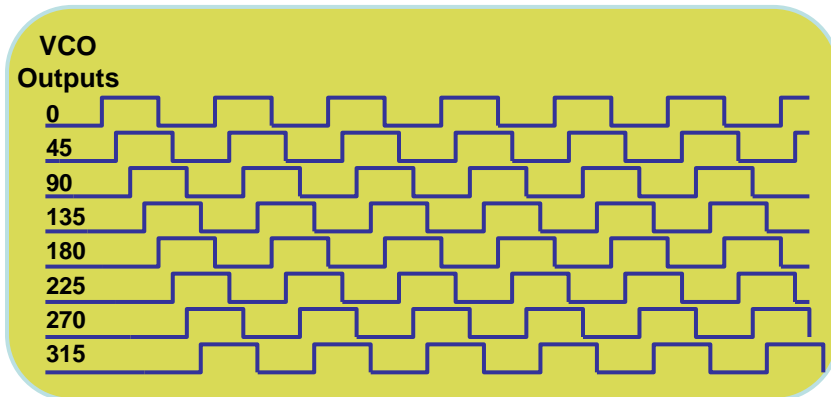
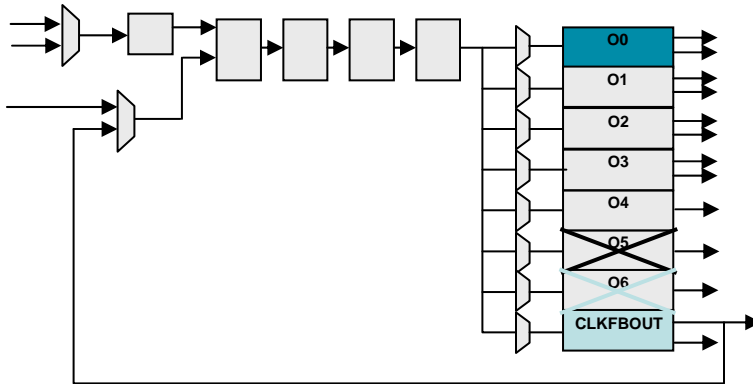
Complements external PLLs, lowers system cost

- **Many possible inputs to each MMCM**
  - CCIO from inner IO columns
  - Global clock inputs
  - BUFG
  - GTX clocks
  
- **MMCM outputs drive**
  - BUFG
  - BUFH in same region
  - Performance Paths to BUFIO and BUFR

Clock Capable IO can drive MMCM and BUFG directly



VIRTEX



Signals can be phase-shifted in relation to each other

■ **Fractional counters**

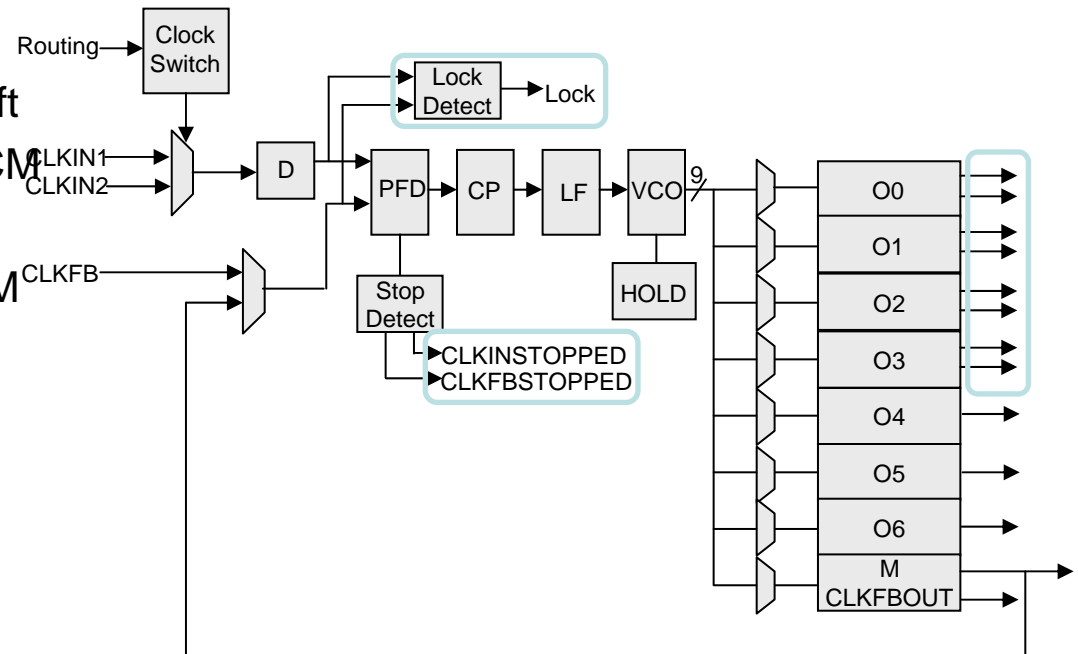
- Ability to configure O0 and CLKFBOUT as counters with 1/8<sup>th</sup> granularity (e.g. 2.125, 2.250, 2.375 etc.)
- O0 and O5 counters can be combined
- CLKFBOUT and O6 counters can be combined
- Enables many more frequencies to be synthesized

■ **Two methods of shifting phase**

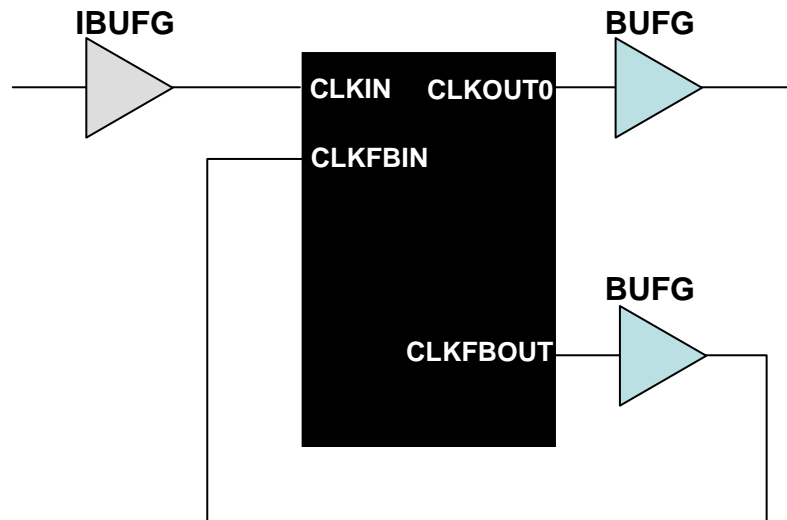
- Static Phase Shift using time-shifted VCO outputs

- Dynamic Phase Shift using the PS port to change the phase on the fly in increments

- **Complement outputs**
  - O0-O3 of every MMCM have both True and Complement outputs
  - Provide 180 degree phase shift
  - Enables porting of Virtex-5 DCM
- **LOCKED**
  - Signal showing that the MMCM has locked on to the input frequency
- **CLKINSTOPPED/FBSTOPPED**
  - Status signals, indicating that the input or feedback clocks have stopped running
- **PWRDWN**
  - Disable / Enable signal to the regulated supply of each MMCM



Additional signals to make the MMCM a powerful system component



- **Precise phase relationship between input clock and output clock**

- Most flexible solution but requires two global clock buffers
- Used in Source Synchronous and System Synchronous applications

- **CLKIN frequency must match CLKFBIN frequency**

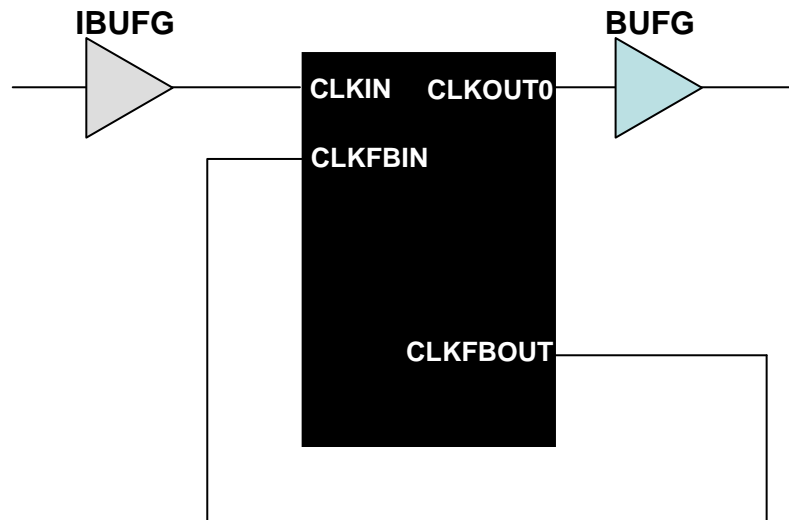
- i.e.  $F_{in}/D = F_{vco}/M$

- **Example:**

- $F_{in}=250\text{ MHz}, D=1, M=3, O=1$

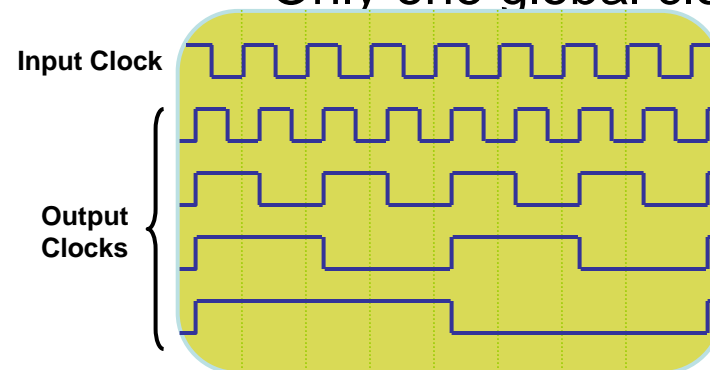
Controlled phase relationship between input clock and output clock

–  $F_{in}/D = F_{vco}/M = 250\text{ MHz}$

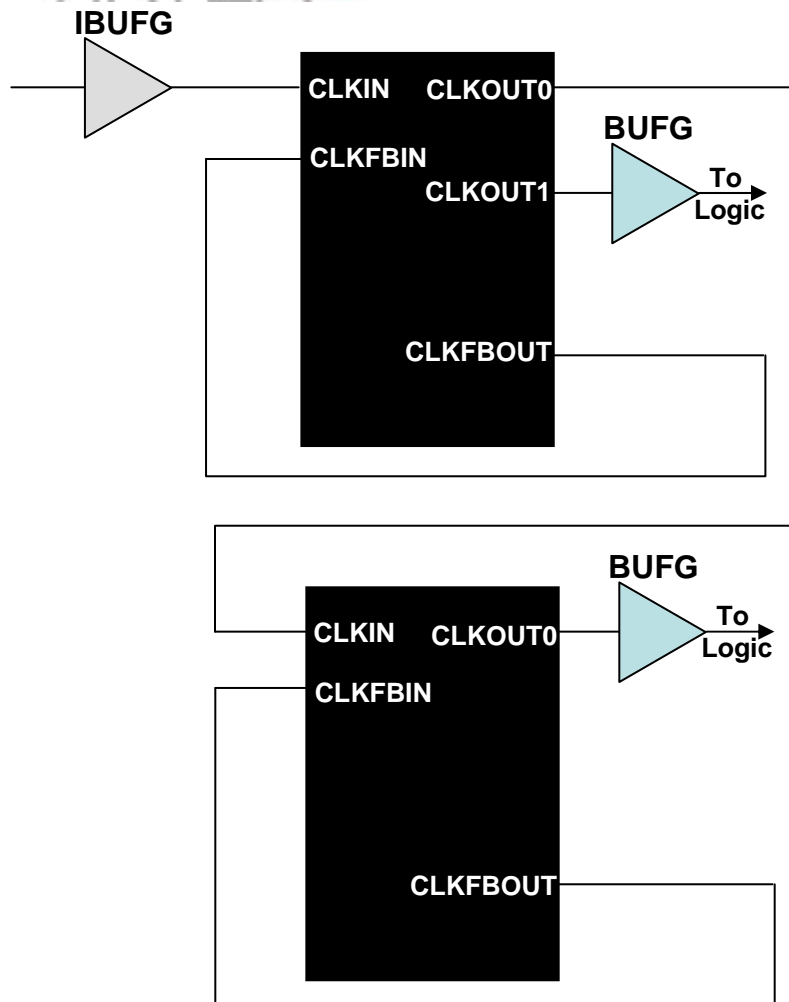


- **When a controlled phase relationship between input clock and output clock is not required**

- MMCM used only as frequency synthesizer or jitter filter
- Only one global clock

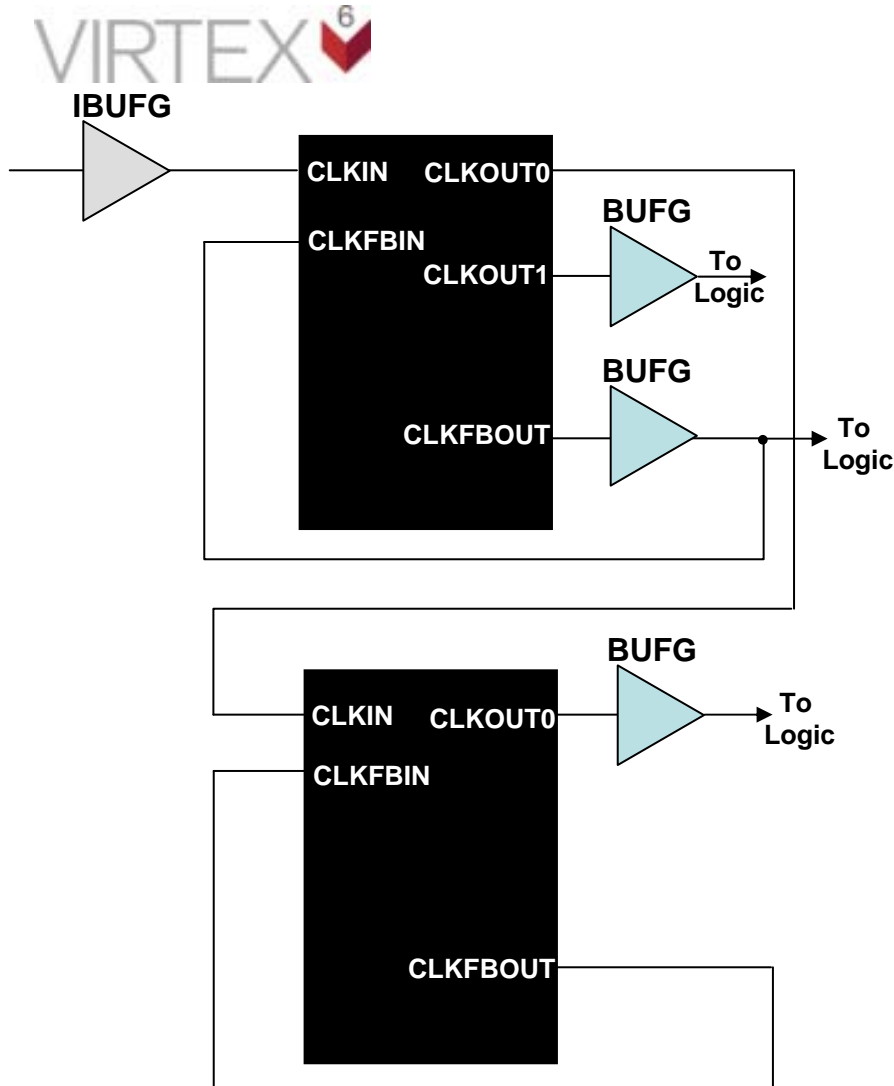


Limiting functionality to frequency synthesis or jitter filter saves one global buffer



- **MMCM in the same CMT can be connected without the need for a global clock buffer**
  - Output clock will not be aligned to input clock
- **More clock frequencies can thus be generated**

Dedicated connection between MMCM in CMT saves a global clock buffer



- **MMCM in the same CMT can be connected without the need for a global clock buffer**
  - Output of first MMCM connected to CLKFBIN of second MMCM
  - BUFG inserted from CLKFBOUT to CLKFBIN of the first MMCM to align output clock with input clock
  - CLKFBOUT of first MMCM can also drive logic
- **More phase-aligned clock frequencies can thus be generated**

Large number of phase-aligned clock frequencies can be generated

**Step 1:**

- Select desired MMCM features
- Enter input frequency and jitter requirements

**Step 2:**

- Choose number of output clocks
- Select frequency, phase and duty cycle of all output clocks

**Step 3:**

- Select input clock buffer source, output clock buffers
- Choose which optional pins to use and specify the feedback path

**Step 4:**

- Review / edit settings (Bandwidth, Compensation)
- Review / edit values (period, jitter, phase)

**Step 5:**

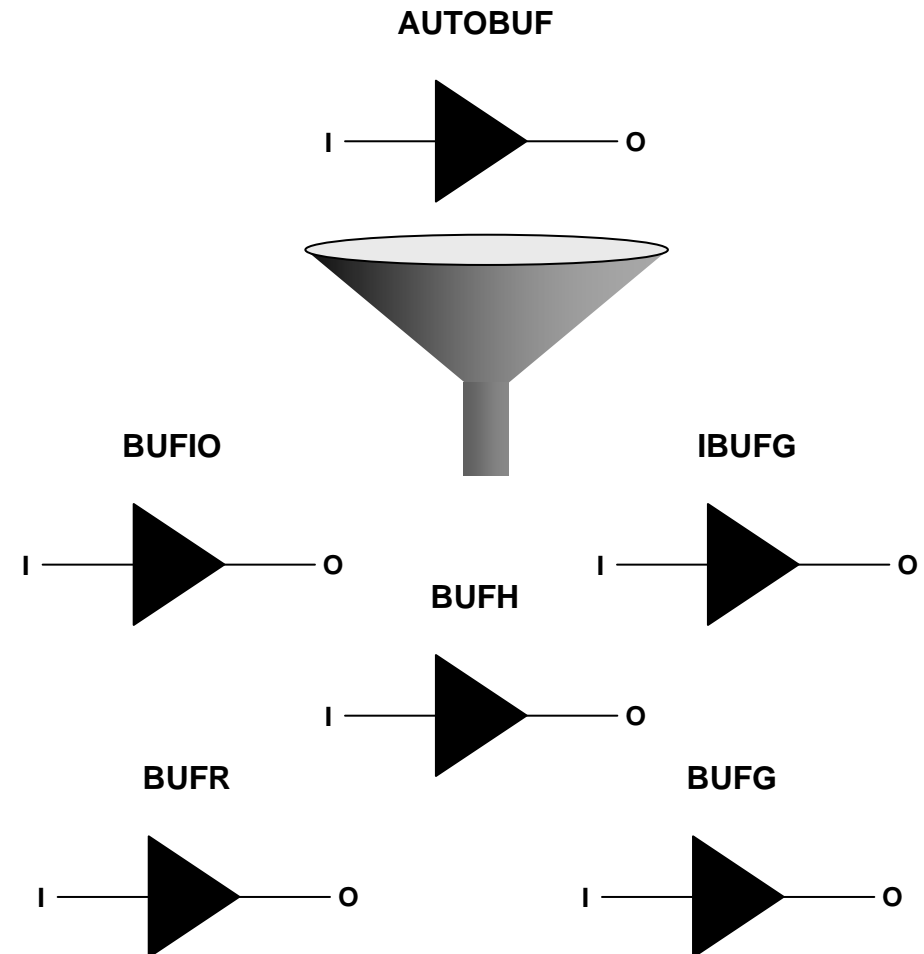
- Review summary of MMCM configuration prior to generating design

**Step 6:**

- View resource summary, XPower parameters and generated files

Simple steps give the user full control

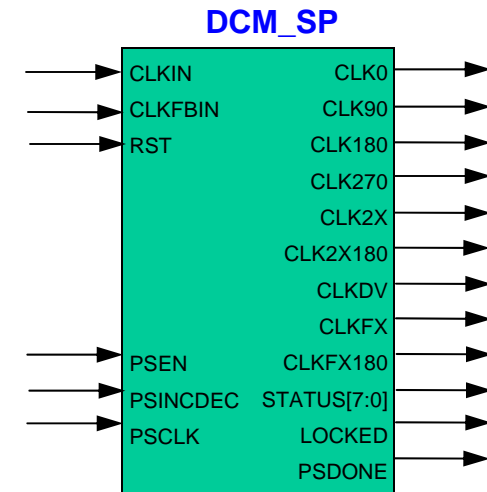
- **AUTOBUF is a simple buffer to be used in place of all clock buffers**
  - Software makes the right buffer choice
- **Single-input buffers only**
  - Cannot invoke buffers with **clock enable**, **frequency divide**, or **select** ports
- **Can be overridden with Buffer\_Type attribute**
  - Gives the user control over implementation if needed



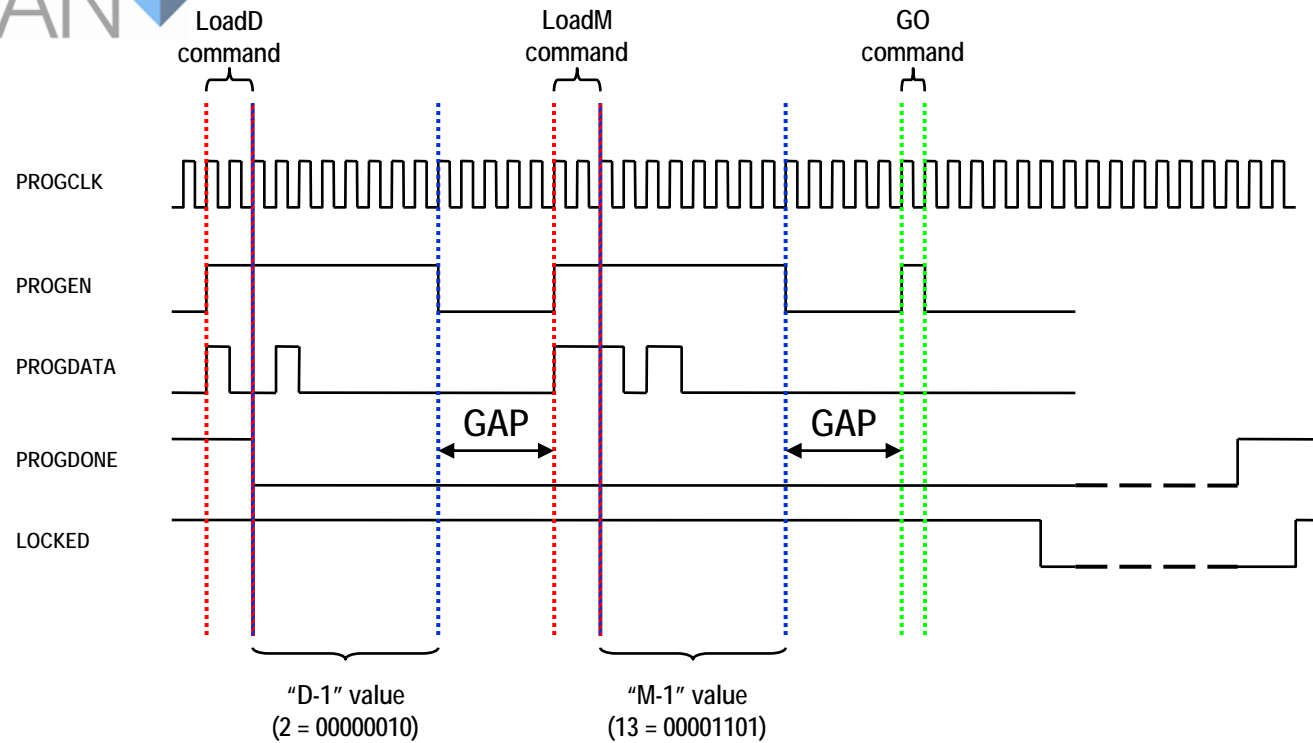
Simplifies clock buffer choice

	Virtex-5	Virtex-6
Number of Clock Regions	8-24	6-18 (double size) <sup>1</sup>
Global Clock Buffer Maximum Frequency (BUFG)	710 MHz	800 MHz
Regional Clock Buffer Maximum Frequency (BUFR)	300 MHz	500 MHz
IO Clock Buffer Maximum Frequency (BUFIO)	710 MHz	800 MHz
Horizontal Global Clock Buffer (BUFH)	No	12 per region
Low-Jitter Path to IO (Performance Path)	No	4 per IO Column per region
Clock Gating Options	32 BUFGCTRL	32 BUFGCTRL and up to 216 BUFHCE <sup>2</sup>
Global Clock Capable IO	20 GC pins	8 GC pins and up to 72 CCIO <sup>3</sup>
Clock Management Tile	Two DCM and one PLL	Two MMCM
CMT per device	Up to 6	Up to 9
VCO Maximum Frequency	1440 MHz	1600 MHz

- **Provides access to traditional clock management features**
- **DLL**
  - On-chip de-skew
  - Phase shift (fixed or variable)
- **DFS**
  - Static Frequency Synthesis
- **Can tolerate incoming spread spectrum clock**
  - Refer to XAPP469
- **Automatic frequency search**
  - No need to explicitly set LOW/HIGH\_FREQUENCY\_MODE for both DLL and DFS
  - Same as in Spartan-3A but different from Virtex-5

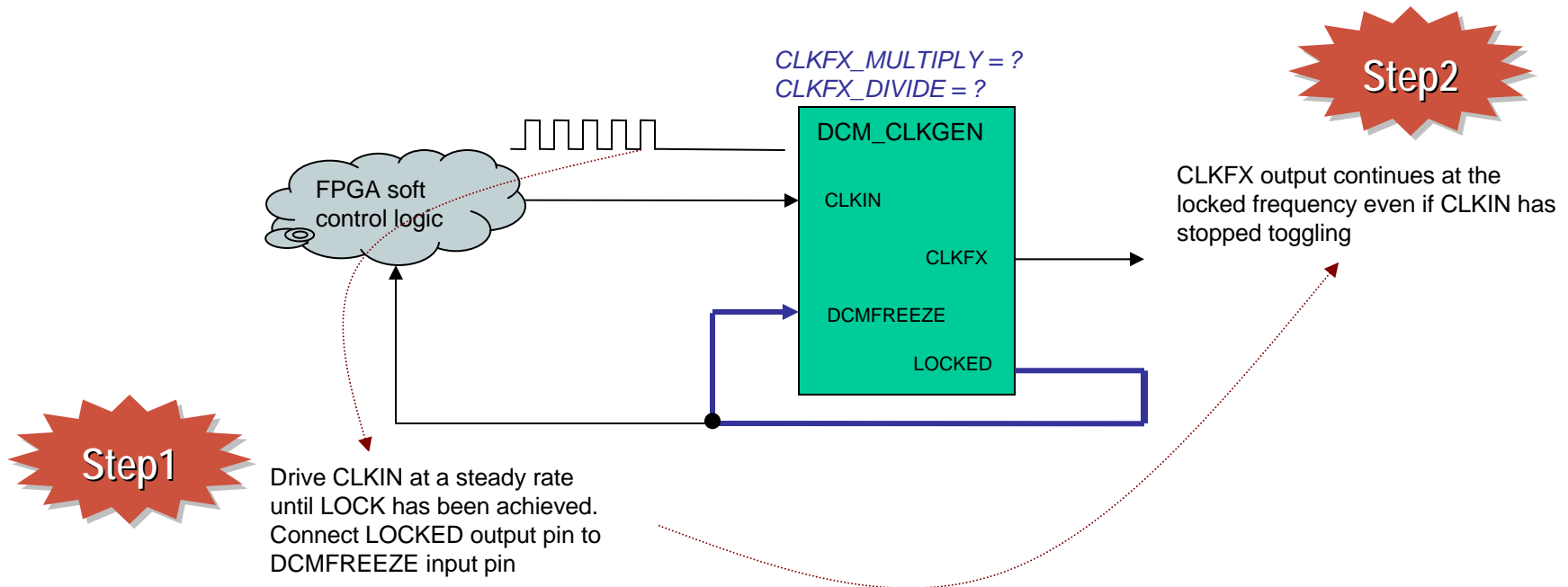


***Retained DCM functions from Spartan-3A, including both DLL and DFS***

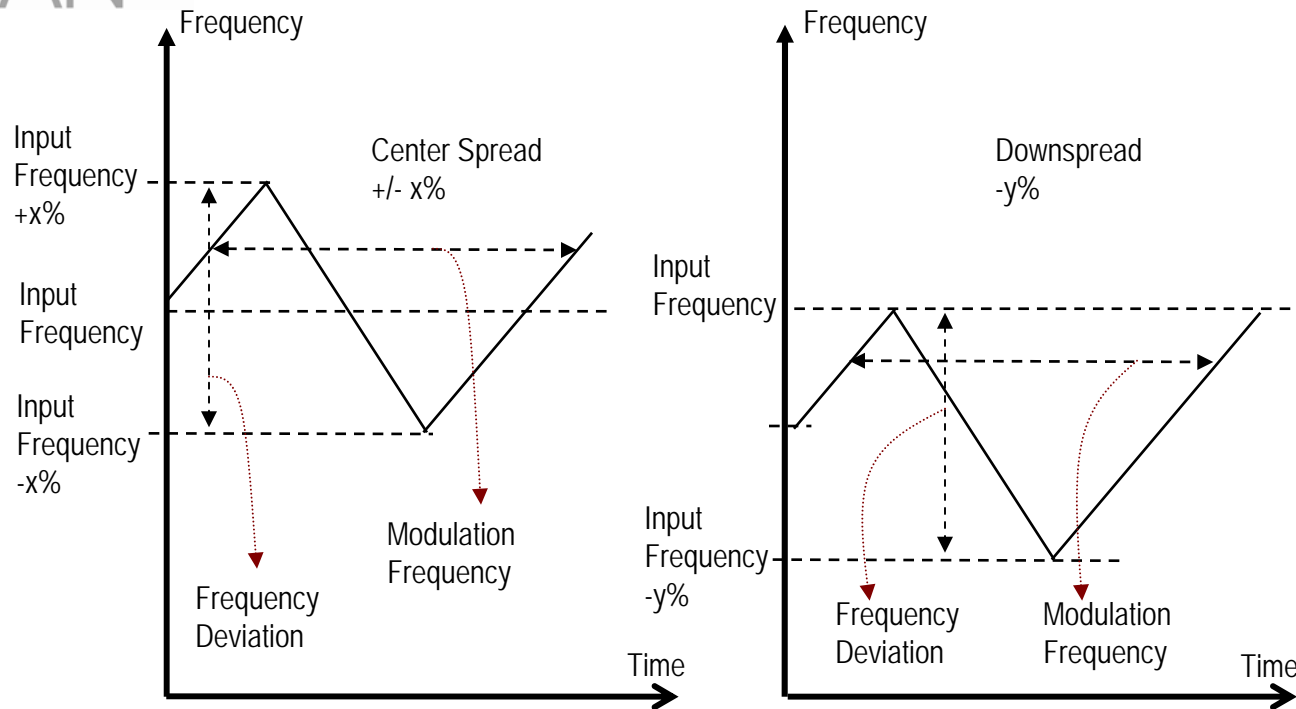


- **Lock time depends on**
  - PROG\_MD\_BANDWIDTH attribute setting (see User Guide for further reference)
  - The magnitude of the frequency change

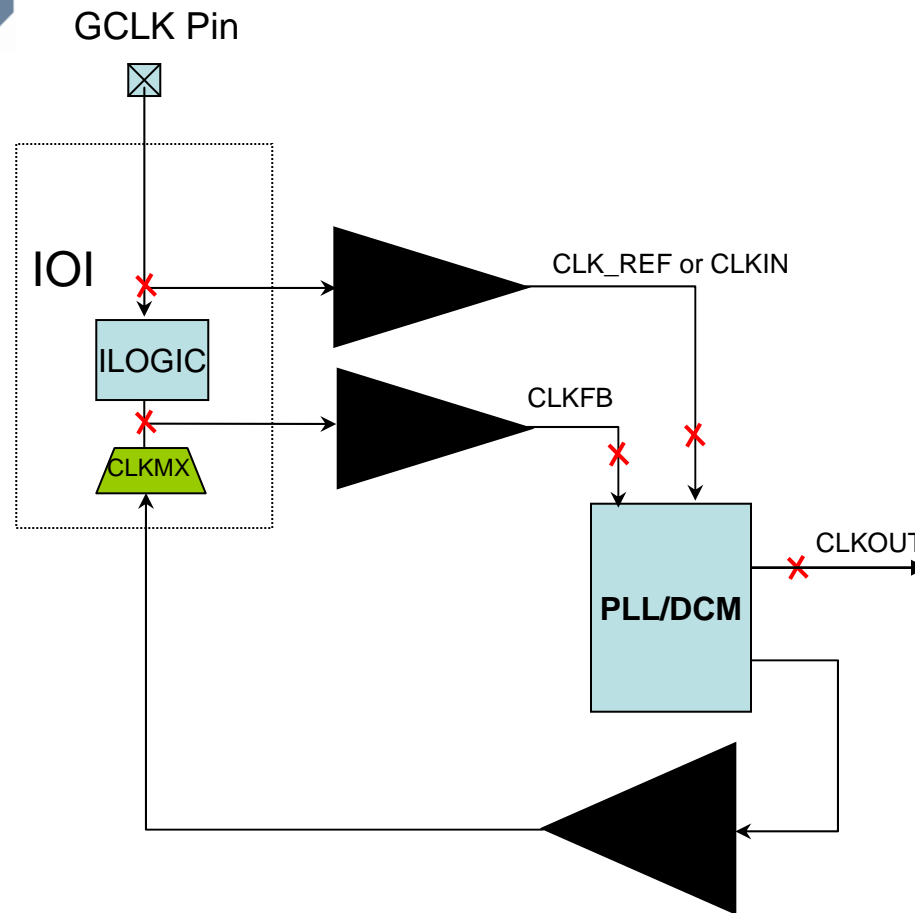
**Three SPI commands to change M/D on-the-fly**



**DCM Freezes: Used as a free running oscillator**



- **Three spread spectrum modes are supported**
  - 24 MHz (input frequency), down-spread (amplitude y to be characterized), triangular modulation
  - 75 MHz (input frequency), center-spread (amplitude x to be characterized), triangular modulation
  - 90 MHz (input frequency), center-spread (amplitude x to be characterized), triangular modulation



***BUFIO2FB is added to match clock routing delays between CLKIN and CLKFB  
Software automatically inserts the buffer without need for user attention***